New Hot-Carrier Degradation Mechanism for MOSFET Devices Using Two-Type Interface-State Model

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Abstract

We have studied the characteristics of MOSFET degradation induced by hot-carriers. When the characteristics of drain current degradation (ΔI_d) are applied to the stress time(t) dependence $\Delta I_d \propto t^n$, the exponent n is clearly different under different bias conditions. We present a two-type interface-state model composed of deep-energy interface states and shallow-energy interface states which have a different n exponent in order to explain the characteristics of drain current degradation.

1. Introduction

One of the most important reliability issues in deep-submicron MOSFET devices is the hot-carrier-induced oxide damage which results in drain current degradation. There are several drain current degradation models [1, 2] which are used in MOSFET hot-carrier reliability simulation. Most of them are expressed as:

$$\Delta I_d(t) \propto \Delta N_{it}(t) \propto t^n, \tag{1}$$

where ΔI_d is the drain current degradation, N_{it} is the interface-state density, and t is the stress time. Although this equation assumes a constant exponent n under the same stress condition, as shown in Fig. 1 this exponent is clearly different under different bias conditions. The exponent n mainly depends on the gate voltage, as shown in Fig. 2.

2. Two-Type Interface-State Model

In order to explain this gate voltage dependence of exponent n, we present a new interface-state model called the two-type interface-state model. In this model, two types of interface states are assumed. One is the deep interface state, which exists in the bandgap and correspond to the conventional model; the other is the shallow interface state, which exists in the conduction band. These two-types of interface states have different n exponents in Eq. 1. The exponent of the deep interface state is n_d and that of shallow interface state is n_s. n_s is assumed to be smaller than n_d. As shown in Fig. 3, when the gate voltage is low, electrons are trapped only in a deep interface state. As the gate voltage is increased, which means that the Fermi level is higher, some electrons begin to be trapped in a shallow interface state. As a result,

the total exponent n of the interface states is between n_d and n_s and is smaller at higher gate voltages, as shown in Fig. 2.

Figure 4 shows the interface-state spatial density distribution obtained from charge-pumping measurement. Only the deep interface states are observed by charge-pumping measurement[3]. Therefore, the calculated drain current degradation, which is obtained by using the interface states in Fig. 4, is smaller than the experimental one, particularly in the high gate voltage region. Then the shallow interface-state energy distribution is decided in order to fit the characteristics of drain current degradation of the experiment in the high gate voltage region. Figure 5 shows the interface state energy distribution which includes the shallow interface states. The distribution has also been obtained from several other experiments [4, 5]. In the two-type interface-state model, the interface-state density distribution $N_t(x,\varepsilon,t)$ is expressed as:

$$N_t(x,\varepsilon,t) = f(x)D(\varepsilon,t)$$
$$D(\varepsilon,t) = \begin{cases} D_d t^{n_d} & (\varepsilon < \varepsilon_c + \Delta\varepsilon) \\ D_d t^{n_d} + D_s t^{n_s}(\varepsilon - \varepsilon_c - \Delta\varepsilon)^{\alpha} & (\varepsilon \geq \varepsilon_c + \Delta\varepsilon), \end{cases} \quad (2)$$

where $f(x)$ is the stress-induced interface-state spatial density distribution obtained from charge-pumping measurement, $D(\varepsilon,t)$ is the density of interface states, ε_c is the bottom of the conduction band, D_d and n_d are the deep interface-state's parameters, D_s, $\Delta\varepsilon$, n_s and α are the shallow interface-state's parameters, and x, ε, and t are the lateral location from the gate center, energy, and stress time, respectively. The drain current degradation is calculated by the device simulator by considering the interface-state distribution of Eq. 2.

3. Results and Discussion

As shown in Fig. 6, the drain current degradation using the conventional interface-state model is lower than the measurement in the high drain region, but the degradation using the two-type interface-state model agrees well with the measurement. The two-type interface-state model satisfactorily represents the stress time and the gate voltage dependence of the drain current degradation (Figs. 7,8).

4. Conclusion

We presented the two-type interface-state model using Eq. 2 from the characteristics of MOSFET degradation induced by hot-carriers. The model satisfactorily represents the stress time dependence of the drain current degradation under several bias conditions.

5. Acknowledgement

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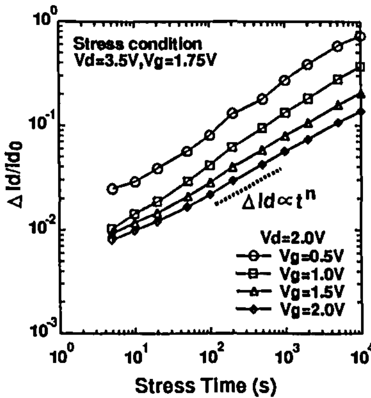

Fig. 1: Stress time dependence of the drain current reverse-degradation. I_d was measured at $V_d = 2V$.

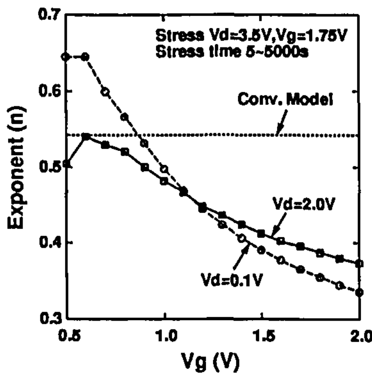

Fig. 2: Gate voltage dependence of reverse-degradation exponent n. The dashed and solid lines are from measurements at V_d=0.1V and V_d=2.0V, and the dotted line is from the conventional interface-state model.

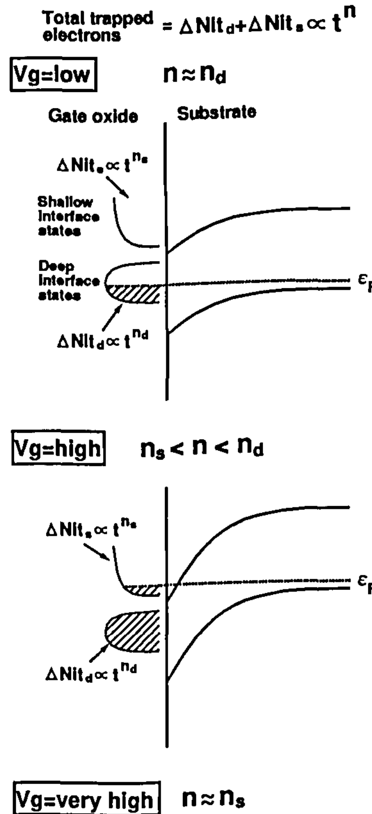

Fig. 3: Schematic diagram of the two-type interface-state model and gate voltage dependence of degradation exponent n.

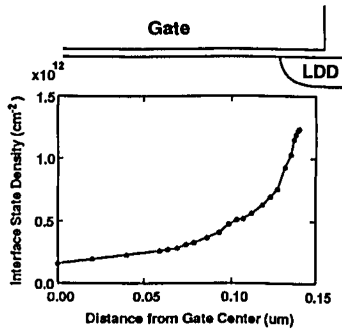

Fig. 4: Interface-state spatial density distribution generated by hot carriers. This distribution was obtained from charge-pumping measurement.

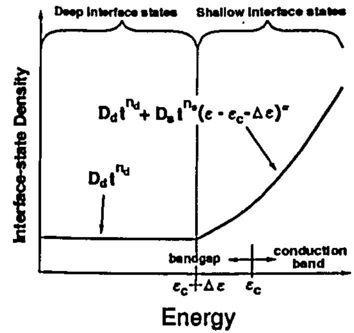

Fig. 5: Interface-state energy distribution (Eq. 2) of two-type interface-state model.

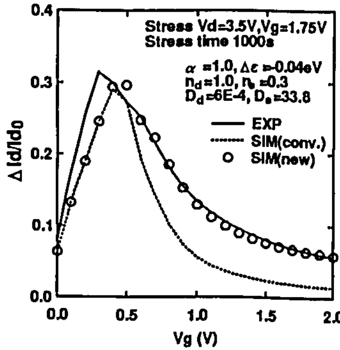

Fig. 6: Drain current reverse-degradation rate versus gate voltage. Open circles are from measurements, the dotted line is from the conventional model, and the solid line is from the two-type interface-state model.

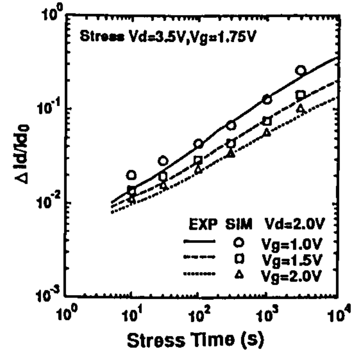

Fig. 7: Stress time dependence of drain current degradation. I_d was measured at $V_d = 2V$.

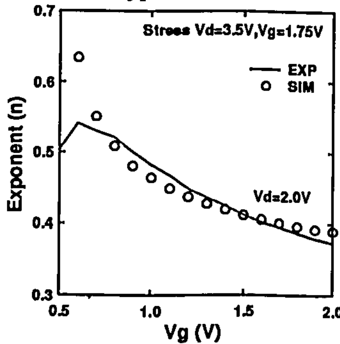

Fig. 8: Gate voltage dependence of reverse-degradation exponent n. The solid line is from measurements and the open circles are from the two-type interface-state model.