Modeling the trapping and de-trapping of phosphorus at the Si to SiO_2 interface

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Abstract

The phosphorus dose loss by trapping at the Si-SiO_2 interface was studied for the various process modules of a 0.3 μm CMOS technology, both separately and in combination. SIMS measurements showed significant dose loss, up to 30%, and also a sizable de-trapping after a 1000°C anneal. The de-trapping was observed as an additional peak at the silicon surface. A new model which includes both trapping and de-trapping phosphorus fluxes was incorporated into the process simulator PROPHET. Subsequently, simulations were able to reproduce the SIMS data as well as NMOS threshold voltage values. The model also showed that the dose loss is enhanced by TED, thereby explaining the measured dependence of the dose loss on the implanted dose, and the fact that the major dose loss in the CMOS process occurred during the first anneal after implantation.

I. Introduction

Motivated by recent experimental works [1-4], we had developed previously a simple model for the trapping of phosphorus at the Si to SiO_2 interface which gave rise to a phosphorus dose loss from the silicon. The model worked well for simulating the device characteristics of CMOS devices and isolation structures [5]. However, it did not account for the de-trapping effect, observed in [1] following 1100°C Rapid Thermal Anneal (RTA). Nonetheless, it illustrated the importance of the phenomenon and prompted the present further investigation and a more complete model. In this study, wafer splits were designed using process modules of a 0.3 μm CMOS technology as building blocks, so that the effects of different technologically-relevant anneal cycles could be isolated, including a 1000°C RTA step.

II. Experiment and Results

A 150Å screen oxide growth was followed by a 60 keV phosphorus implant at a dose of either 3.2×10^{12} or $3.2\times10^{13}cm^{-2}$. The subsequent optional steps were: screen oxide etch, 55Å gate oxidation (GOX) at 850°C, 900°C inert Furnace Anneal (FA), 800°C dry oxidation FA, 875°C inert FA, 1000°C 10s RTA. Fig. 1 summarises the results for the total phosphorus dose remaining as measured by SIMS (Secondary Ion Mass Spectroscopy), performed after etching of any remaining oxide with a 14.5keV Cs primary beam. With the exception of the wafers with low implant dose and hence a smaller Signal-to-Noise ratio, all other splits show an increase of the remaining dose after RTA, i.e. there is significant de-trapping of phosphorus at 1000°C. The de-trapping appears as an additional peak in the doping profile close to the surface, as shown in Fig. 2(a)-(d).

III. Model

Our new model has two flux terms: (1) a trap flux, similar in form to that in our previous work[5]:

$$F_{trap} = r_T C_P^I (1 - Q_{trapped} / Q_{sites}) \qquad (1)$$

and (2) a de-trap flux:

$$F_{detrap} = r_D Q_{trapped} / t_{trap} \qquad (2)$$

where r_T and r_D in μms^{-1} is the phosphorus trap and de-trap rates, C^I_P in cm^{-3} is the active phosphorus concentration in silicon at the interface, $Q_{trapped}$ and Q_{sites} are the areal concentrations of the trapped dose and trap sites at the interface in cm^{-2}, and t_{trap} is the thickness of the layer of trapped phosphorus, assumed to be 1.5Å. The rates r_T and r_D are assumed to have Arhenius expressions, and their values chosen to give the best fits. This model is incorporated into the process simulator PROPHET [6], and simulations employed the dose loss model with fully-coupled diffusion, assuming initial net interstitial distribution to be a modified "+1" model [7], with 1.35 net interstitial for each implanted dopant ion as extracted from IMSIL Monte-Carlo simulation [8]. For the oxidation steps, a segregation coefficient of 10 is assumed for phosphorus at the Si-SiO_2 interface [10].

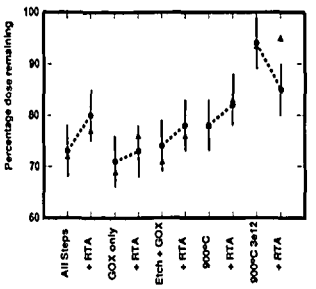

Figure 1: Total dose remaining, as a percentage of the implant dose, versus processing conditions. Data measured by SIMS are circles, with +/- 5% error bars estimated from a prior boron dose calibration [9]. Simulated data are triangles. Dashed lines show the measured change due to an additional 1000°C RTA. Implant dose was $3.2x10^{13}cm^{-2}$, except for the last two splits as marked above.

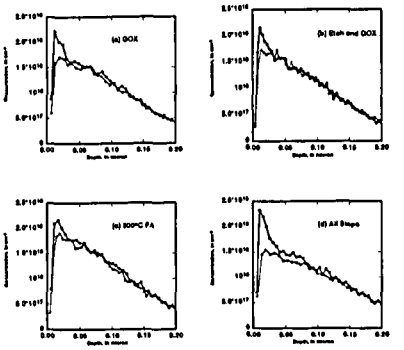

Figure 2 Effect of a final 1000°C RTA on the doping profiles of wafers implanted with 3.2e13 cm^{-2}. Open (closed) circles show SIMS-measured profiles before (after) RTA for splits with (a) gate oxidation(GOX) only, (b) screen oxide etch and GOX, (c) 900°C anneal, and (d) all steps described in the text.

IV. Modeling Results

Fig. 3 shows the variation of threshold voltage (Vth) for a series of NMOS devices which were counter-doped to achieve very low Vth values. In the case of arsenic as the counter-doping specie, the trend of Vth with respect to the counter-doping implant dose is well simulated when an arsenic trapping model previously developed [11] was used. For the case of phosphorus, the Vth trend can be well simulated with either (a) our previous model which includes only the trapping flux, or (b) the new model with both trapping and de-trapping flux. We note that the maximum temperature in the NMOS fabrication is 900°C. In contrast, when phosphorus trapping is ignored, the simulated Vth values are lower than measured values by as much as 0.75V. Fig. 4 shows the as-implanted and final SIMS profiles of the wafer which underwent all the CMOS processing except for RTA, i.e. maximum processing temperature is 900°C. We note that for the purpose of comparing with SIMS profiles, all simulated profiles were convolved with the broadening due to the knock-on effect of the SIMS primary beam. The simulation without phosphorus trapping overestimates the doping, while simulation with an infinite trapping rate (corresponding to unity sticking coefficient)

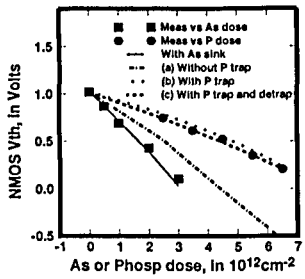

Figure 3: NMOS Vth as a function of the counter-doping implant dose. The simulations for As counterdoping (solid) used the trapping model of [11]; for phosphorus, three sets of simulations are shown a) without trapping (stipple) (b) with a tuned trapping rate (dots), and (c) with trapping and de-trapping (dashes).

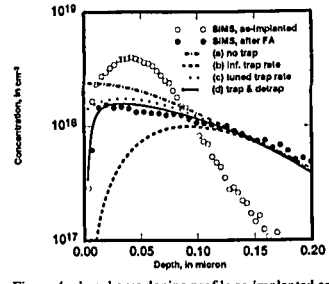

Figure 4: phosphorus doping profile as-implanted and after all furnace anneals, by SIMS measurement (symbols). The final profile is also simulated (lines) (a) without trapping, (b) with infinite trapping rate, (c) with tuned trapping rate, and (d) with both trapping and de-trapping rates.

underestimates it. Simulations (c) with trap flux only, and (d) with both trap and de-trap fluxes, where the trap/de-trap rates' parameters were chosen to give good fits to the device results, both show good fits to the SIMS profile. Thus, when the processing temperatures are 900°C and below, both the trap models work well.

Fig. 5 shows the SIMS profile before and after the 1000°C RTA for the splits with all anneal steps. The observed extra peak due to de-trapping could only be reproduced with the new trap & de-trap model, in contrast to the cases at lower processing temperatures.

Fig. 6 compares the doping profiles after the 55Å GOX process, with and without 150Å screen oxide etch. The latter split thus experienced little oxide growth after the phosphorus implant. Both SIMS and simulated profiles show little difference between the two splits, demonstrating that the trap/de-trap fluxes are independent of the segregation flux during oxidation, as assumed in our model.

Fig. 7 compares the doping profiles after a 900°C anneal for implant dose of 3.2×10^{12} and 3.2×10^{13} cm^{-2}. Not only is the Transient Enhanced Diffusion (TED) obviously much larger in the higher dose case, as expected, but the dose loss is also larger (remaining dose is 78% vs. 94% for the lower dose). The data strongly suggests that the dose loss occurs with TED and not during any earlier process, for instance migration of interstitial dopant atoms left by implantation. The simulations follow the observation because more TED leads to more phosphorus pile-up at the surface [6], and hence more phosphorus trapped. Table 1 illustrates this point further by detailing the amount of total dose remaining after each anneal, showing that most dose loss occurs in the first anneal after implant, which is GOX, when TED is greatest. The same can also be deduced from Fig. 1 which shows that the dose loss for the wafer with GOX only is almost identical to that for all steps, for measured and simulated data. Finally, Fig. 1 also compares the simulated and measured total dose remaining: with the exception of one data point which has a low Signal-to-Noise ratio and is inconsistent with the general trend, for all other data points simulations agree with SIMS.

V. Conclusion

The phosphorus dose loss effect has been studied using process modules of a 0.30 μm CMOS technology. Results show that the de-trapping effect is significant at 1000°C. An improved model which includes both trapping and de-trapping of phosphorus is able to fit both the measured doping profiles and

device Vth well, and shows that the dose loss occurs mainly during the processing steps with large TED.

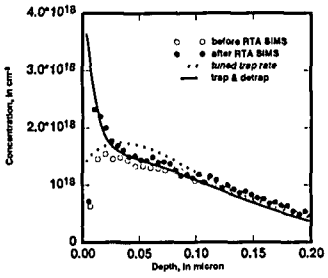

Figure 5: Final phosphorus doping profiles after all furnace anneals (open circles) and after an additional RTA (closed circles) as measured by SIMS. The profile after RTA is simulated with trapping only (dots) and with both trap and de-trap (solid).

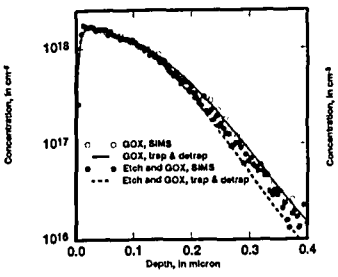

Figure 6: Measured and simulated P doping profiles after GOX only, and after screen oxide etch and GOX. The difference in processing yielded little difference in doping profiles.

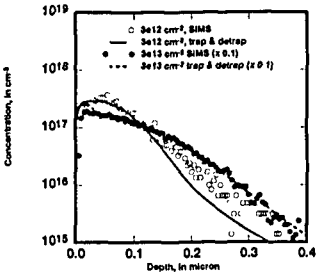

Figure 7: Measured and simulated phosphorus doping profiles of wafers implanted with $3.2x10^{12}$ or $3.2x10^{13}$ cm^{-2}, and subjected to 900°C FA only. The higher dose profiles are scaled by 0.1.

VI. References

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Table 1: Simulated dose loss after each anneal cycle

Process	Total dose
Gate oxidation steps:	
700°C soak	95%
ramp-up	73%
850°C oxidation	72%
ramp-down	71%
900°C FA	78%
800°C FA	72%
875°C FA	72%
1000°C RTA	77%