A Physically-Based Compact Model for LDMOS Transistors

James Victory[a], Colin C. McAndrew, Rainer Thoma, Kuntal Joardar, Margaret Kniffin, Steve Merchant, Diana Moncoqut

Motorola, Inc.,

[a]207, Route de Ferney, P. O. Box 15, 1218 Le Grand-Saconnex, Geneva, Switzerland

Abstract

This paper presents a physically based model for LDMOS transistors. The model advances the state-of-the-art by using a formulation applicable across a wide voltage range, by accounting for the distributed parasitic metal effects, and by properly modeling the bias dependence of parasitic capacitances. The model is implemented in Motorola's internal simulator MCSPICE.

1. Introduction

LDMOS (lateral double-diffused MOSFET) transistors have emerged as the preferred smartpower control devices, providing voltage blocking capability from low (~15V) to very high (~1000V) voltages [1,2]. Proper design of smartpower ICs, requires accurate circuit level modeling of LDMOS. This work presents a new, physical, accurate LDMOS compact model, to address this need. Fig. 1 shows a 25V LDMOS cross section, from Motorola's SmarTMOS™ technology. Although this device is the main subject of the paper, the model presented has been used for very high voltage (700V) LDMOS where the NEPI is replaced by a deep diffused NWELL. In the sections following, each region of the device is discussed and the modeling presented. Temperature dependence, parasitic diodes and metal overlap capacitances are not presented here.

2. Graded Channel

The difference between the PHV and NSD lateral diffusion fronts forms the bulk/channel region of the LDMOS. The two most relevant effects in LDMOS is the sharp peaking of the transconductance (g_m) at threshold and the increase of the gate-to-drain capacitance well below threshold (section 6). Previous LDMOS models assume uniform lateral channel and thus can not reproduce such effects [3]. In this work, the channel model is a physically based graded channel charge sheet model GCIM (Graded Channel IGFET Model) which is implemented in Motorola's simulator MCSPICE [4]. The basic principle of graded channel charge sheet models has been reported by Victory *et. al.* [5]. The channel is partitioned into regions of uniform doping. Current and charge expressions in each region are derived from charge sheet principles and given in their entirety by Joardar *et. al.* [6].

3. Accumulation (poly overlap of NEPI)

In normal operation, positive gate bias attracts electrons to the surface, forming a highly conductive accumulation layer. The equation for the current is given by

$$I_{ac} = \frac{\mu_{ac} C_{ox} W_g}{L_{ac}} \cdot \frac{(V_{gch} - V_{fb})}{(1 + \theta_{ac}(V_{gch} - V_{fb}))} \cdot \frac{V_{acch}}{sqrt\left(1 + \left[\frac{V_{acch}}{E_{cr} L_{ac}}\right]^2\right)}, \quad (1)$$

where μ_{ac} is the low field mobility, θ_{ac} is the gate field mobility degradation factor, and

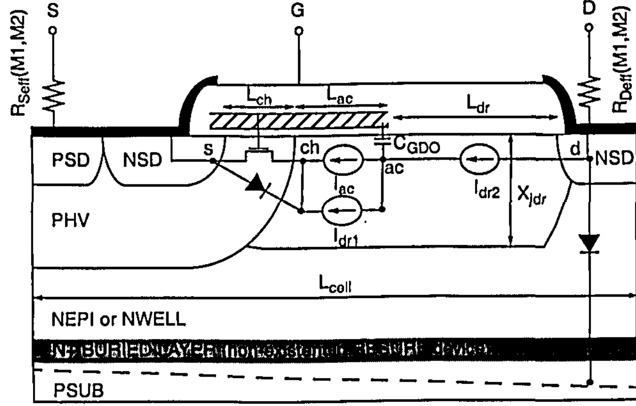

Figure 1: Cross-section of LDMOS including circuit model.

V_{fb} is the flatband voltage. The carrier mobility degradation due to lateral field velocity saturation effects is modeled by the square root term where E_{cr} is the critical electric field for velocity saturation.

4. Drift Region

The NEPI provides a path for current flow I_{dr1} under the gate poly in parallel with I_{ac} and from the poly edge to the drain NSD through I_{dr2}. In both regions, the device behaves as a diffused nonlinear resistor [7]. The drift currents are modeled with the equation

$$I_{dr} = \frac{W_g(X_{jdr} - \alpha\sqrt{\gamma + \overline{V_{sub}}})}{L\rho_{dr}} \cdot \frac{V_{dr}}{sqrt\left(1 + \left[\frac{V_{dr}}{E_{cr}L}\right]^2\right)} \quad , \tag{2}$$

where X_{jdr} and γ are the effective junction depth and built-in potential, ρ_{dr} is the zero-bias NEPI resitivity, α is a doping dependent factor, and E_{cr} is the critical field for velocity saturation. The L and V_{dr} are replaced by the respective region lengths and voltage drops. In NWELL, the depletion pinching effects dominate the nonlinearity, determined by the average junction potentials $\overline{V_{sub}}$. For epitaxial devices, the N+ buried layer absorbs the depletion pinching and X_{jdr} is much smaller than the metallurgical junction depth (see Fig. 1). Fig. 2 displays the model simulated playbacks against data for a device with $W = 80\mu m$, $L_{ch} = 0.9\mu m$, $L_{ac} = 0.2\mu m$, and $L_{dr} = 1.2\mu m$. Good continuous agreement is attained for the drain current and conductances. The peak g_m and the drift region saturation effects (quasi-saturation) are modeled accurately.

5. Metal Resistance

Power LDMOS suffer from parasitic distributed metal resistance effects. Fig. 3 (a) shows a typical layout of an LDMOS, where the device scales with the W_g and n_g (number of gates). The width of the device along each gate is broken up into square cells of length L_{cell}. The cells are connected together by metal 1 to form stripes, which are then connected by metal 2. As the effective width increases, distributed metal resistance effects cause the device scaling to deviate significantly from a simple linear dependence of $n_g \times W_g$. Distributed analysis yields the equations (3-4) for the metal 1 resistance in the drain, where $rcell$ is the cell resistance, $nscm2$ and $ndcm2$ are the number of cells under source and drain metal 2 respectively, and $rd1$ is the metal 1 resistance per cell.

$$\hat{rd} = rcell/nscm2((nscm2\sqrt{rd1/rcell})/(\tanh(nscm2\sqrt{rd1/rcell})) - 1) \tag{3}$$

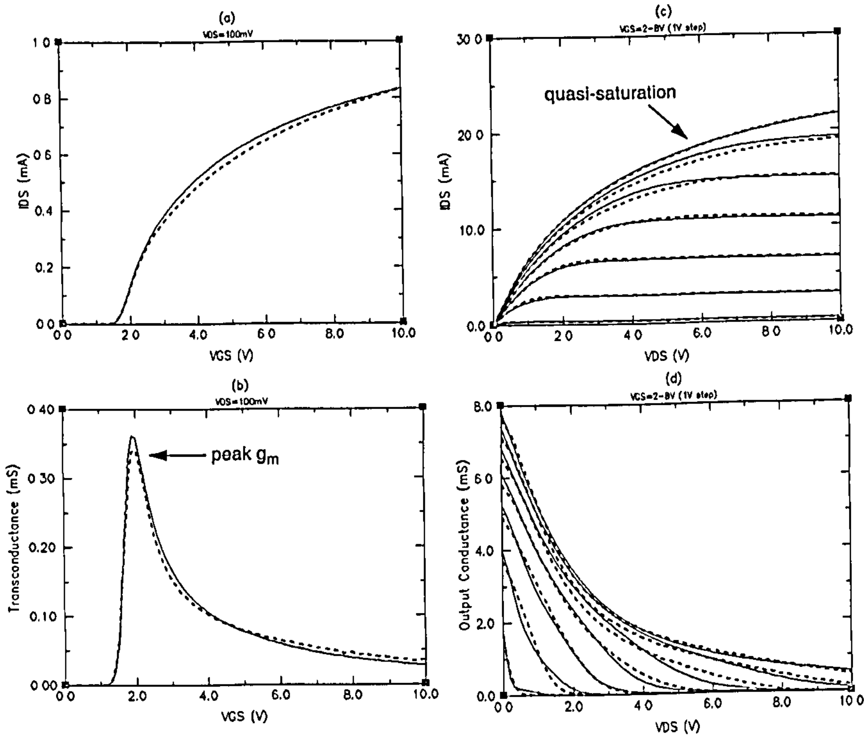

Figure 2: (a) I_{DS} vs. V_{GS}, (b) g_m vs. V_{GS}, (c) I_{DS} vs. V_{DS}, and (d) Output Conductance vs. V_{DS}. All simulated data in solid lines, measured in dashed lines.

$$rd1eff = \left(\frac{nscm2 + ndcm2}{nscm2 + \hat{rd}} \cdot \left(1 + \frac{rcell/nscm2 + \hat{rd}}{rcell/ndcm2 + \hat{rs}}\right)\right)^{-1} \tag{4}$$

Analysis for the drain metal 2 resistance in the drain yields similar expressions. Fig. 3 (b) shows R_{DSon} vs. total gate width for the 25V device, where metal resistance effects account for up to 30% of the total R_{DSon} for large devices.

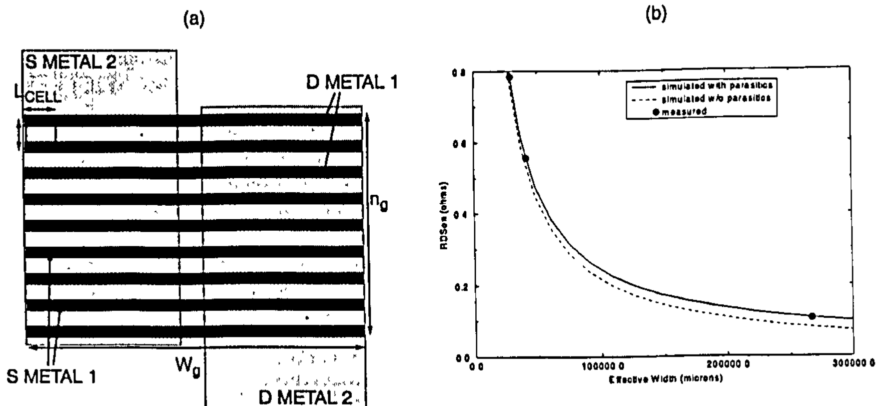

Figure 3: (a) Layout of LDMOS, (b) R_{DSon} vs. effective gate width ($n_g \times W_g$) for V_{DS} = 100mV, V_{GS} = 10V

6. Gate to Drain Capacitance

The gate to drain capacitance C_{GD} is made up of two components: C_{GDC} (associated with the graded channel) and C_{GDO} (results from the poly gate overlap of the NEPI). The C_{GDO}, given by

$$C_{GDO} = \frac{W_g L_{ac} C'_{ox} \varepsilon_s}{\varepsilon_s + C'_{ox} W_{gd}} \quad , \tag{5}$$

is derived from simple MOS capacitor principles, where W_{gd} is the voltage dependent depletion region width under the oxide. Fig. 4 displays the measured and simulated C_{GD} for a large LDMOS. For large negative V_{GD}, C_{GD} is given by the minimum C_{GDO}. As V_{GD} increases, C_{GDO} increases passing through flatband to the oxide capacitance. Around this transition, the lightly doped drain end of the channel begins to invert resulting in a rise in C_{GDC} from zero. Once the device reaches threshold, the source now supplies charge to the channel and the C_{GDC} reduces. Fig. 4 shows the three section simulated and measured C_{GD}. Measured data above threshold is not shown due to measurement error. The simulated curve is not smooth like the data due to the partitioning of the channel into uniformly doped regions, however, the physical trends are modeled closely.

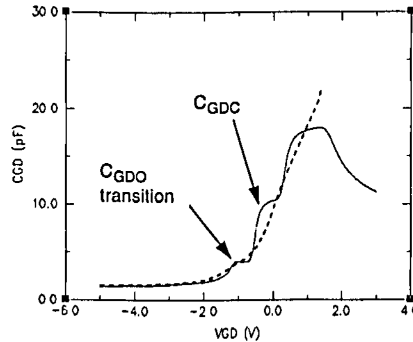

Figure 4: Gate to drain capacitance ($V_S = 0$, $W_G = 360\mu m$, $n_g = 42$)

7. Conclusion

This paper presents a new physically based LDMOS model, the first reported LDMOS model based on a charge-sheet analysis of the graded channel region. In addition, the nonlinear effects of the drift and accumulation regions and distributed metal resistance effects are physically modeled. The model has been implemented in MCSPICE and is currently in use at Motorola for simulation of SmarTMOS™ ICs.

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