Statistical Modeling based on extensive TCAD simulations Proposed methodology for extraction of Fast/Slow models and Statistical models

Eric Vandenbossche[1], George Kopalidis[2], Marnix Tack[1], Wim Schoenmaker[2]

[1] ALCATEL MicroElectronics, Westerring 15, BP9700 Oudenaarde, Belgium
[2] IMEC vzw, Kapeldreef 75, B-3001 Leuven, Belgium

Abstract

Determination of fast/slow models and/or statistical models as a function of process dispersions are very challenging for designing new circuits. The present paper describes a methodology to extract fast/slow models and statistical models based on extensive process/device simulation. Also, AC parameters are extracted such as drain to gate overlap capacitance of MOS transistors as a function of process parameters variations. With the help of Principle Component Analysis, it is possible to get an uncorrelated set of parameter that represent electrical and SPICE parameters dispersions. This leads to a more easy analysis for providing statistical models.

1. Introduction.

It has been demonstrated that a better knowledge of the impact of process technology variations on dispersions of electrical parameters and electrical functionality of circuit is very helpful in process controlability [1]. However, the reverse engineering needed for such analysis is not straightforward by only analyzing electrical parameters dispersions and correlations. As a consequence, the use of TCAD simulation is very helpful since each variation applied to process parameters are known. Then, correlation between electrical and process parameters becomes straightforward. Nevertheless, the analysis supposes a full calibrated input deck in order to get not only qualitative but also quantitative results. Based on this calibration, a Design Of Experiment, DOE, is performed where a set of process parameters with associated limits is chosen. Electrical parameters and BSIM3v3 model parameters are extracted. In addition, AC parameters are also extracted leading to a more accurate simulation of gate propagation delay, Tpd, of a CMOS inverter. With these complete set of statistics, Fast/Slow models and Statistical models will be extracted including correlations with AC parameters.

2. Process description and TCAD calibration.

The present analysis is performed on our 0.5µm CMOS technology. The process flow is as follows. PBL is used to formed the local isolation. Twin retrograde wells are performed with 3 implants for NWELL and 3 for PWELL. The gate oxide thickness is 10nm. The polysilicon gate is 0.33µm thick. Low dose LDD implants are performed before the spacer formation and SD implants follow. A Rapid Thermal

Annealing at high temperature allows to activate SD implants. A TiSi2 silicidation scheme is used to decrease access resistance. Interconnection is based on a planarized triple AlCu metal levels with W as contact and via. The process simulation tool used is IMPACT4 [2,3]. The device simulation tool is ATLAS from SILVACO [4]. The figures 1,2,3 show the TCAD calibration on experimental results. For both NMOS and PMOS transistors, a very good agreement is achieved.

3. Statistical Modeling.

3.1 Methodology

Two main difficulties arise when building a DOE: list of process parameters and definition of upper/lower limits. The list of process parameters has been determined through extensive 1D process/device simulation in order to avoid unexpected dominant or second effect parameters. For 2D simulations of the transistors, additional process parameters are used being related to 2D topology. The limits of each process parameter are chosen with respect to equipment variation and/or in-line measurements during processing (e.g. gate oxide thickness). Table 1 describes the process parameter list with associated limits. For instance, the spacer width limits are not symmetrical in order to take into account spacer over etching dispersion, proximity effect on the etch rate. A Monte Carlo type of design has been chosen with 60 points, and equal probability of each random point within the limits is used.
The outputs for the DOE are Id/Vg/Vb and Id/Vd/Vg set of curves of each split point. Based on these, electrical parameters, E-test, from direct extraction, and BSIM3v3 model parameters, from a batch mode optimization with UTMOST [4], are obtained. In addition, overlap capacitance at 0V bias and area junction capacitance are extracted which are part of AC parameters. The sidewall capacitance is not extracted, so taken as a constant for the statistical analysis. Therefore, it is possible to evaluate Tpd based on ring oscillator simulation.
The methodology for extracting Statistical Models is rather simple since the goal is to provide a list of independent parameter, Principal Component or Factor (based on PCA/PFA techniques), where all the BSIM3v3 parameters values can be derived through simple polynomial equations. Then, Monte Carlo design and Design centring are possible. There is increasing interest in statistical models since it does not suffer from being design application dependent.
The definition of Fast/Slow models, or worst case model, is more difficult since it depends mostly on the design application. Let's consider only digital application where mostly Tpd is a main parameter. Based on dispersions of E-test, BSIM3v3 model parameters and Tpd, it is possible to extract, first, correlations and second PCA/PFA. The definition of fast/slow models is taken as follows: fast is lowest Tpd and slow is highest Tpd. Then, based on worst case values of Tpd, it is possible to get values of PCA/PFA and finally those of BSIM3v3 model parameters. It can appear that some PCA/PFA are not correlated to Tpd, leading to various possibilities to define fast/slow models. As a pragmatic solution, these PCA/PFA are taken to mean values.

3.2 Analysis.

Tables 2, 3 and 4 present the correlation matrix of E-test parameters obtained from the simulations. In addition, correlation values from measurements of about 1200 points (50 lots) are shown. A good agreement is obtained between simulations and experiments. This shows that both the list of process parameters and associated limits can describe the experimental dispersions. This confirms the capability to determine fast/slow models and statistical models based on TCAD simulations.
Figure 4 describes the correlation factors between Idsat, Vth and Tox, Lgate for various gate length. This clearly indicates that Tox is no longer a dominant parameter for the nominal transistor. However, the electrical parameters become more and more dependent on Lgate fluctuation.
Table 5 presents the signature of the influence of process parameters on overlap capacitance at 0V bias obtained from the simulation. It is shown that the dispersion of this capacitance is mostly linked to quadratic effects and interaction terms of process parameters. Nevertheless, the overlap capacitance

fluctuation has a negligible influence on the propagation delay of a CMOS inverter as shown in Table. Also, this later result can only be applied to the present technology under study.

4. Conclusion

The present paper describes a methodology for extraction fast/slow models and statistical models based on accurate process parameter dispersion. Careful attention has been given to include all dominant process parameters. As a first result, a very good agreement is obtained between simulation and experiments. It has been demonstrated that for the nominal device, the gate length fluctuation becomes more and more important leading to a lower sensitivity of gate oxide thickness. In addition, drain to gate overlap capacitance, being part of AC parameters, is analyzed, and its dispersion is a complex function of interactions in between process parameters, such as spacer width with LDD and SD implant dose, but also TEOS spacer deposition temperature that is responsible of the Transient Enhanced Diffusion of the LDD profile under the gate.

References

1. D. A. Hanson et al., IEEE Trans. on Semi. Manuf. Vol.9, pp478.
2. E. Vandenbossche et al., IEDM'95
3. E. Vandenbossche et al., ESSDERC'96
4. SILVACO manual 1997.

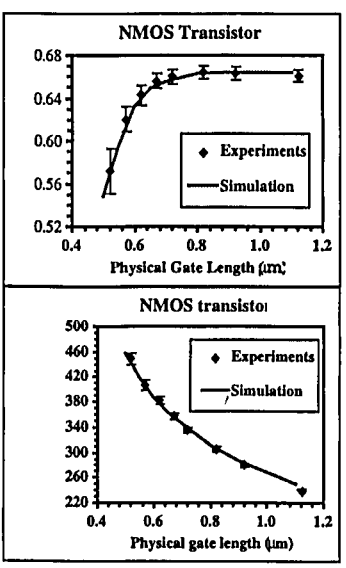

Figure 1 Comparison between simulation and experiments, Vt (top) and saturation current (bottom) for the NMOS transistor. The physical gate length is the one drawn with 0.05µm bias per side.

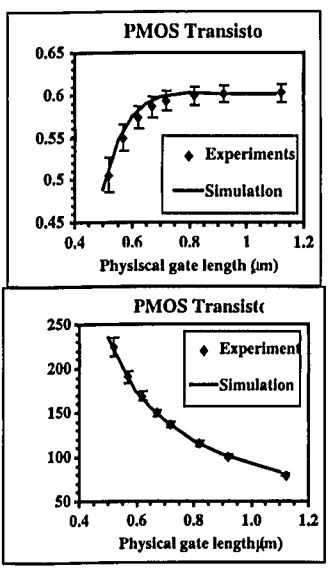

Figure 2 Comparison between simulation and experiments, Vt (top) and saturation current (bottom) for the PMOS transistor. The physical gate length is the one drawn with 0.05µm bias per side.

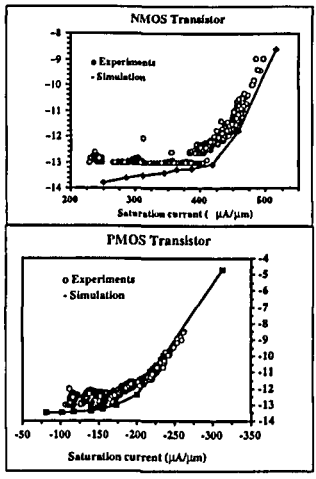

Figure 3 Comparison between simulation and experiments for the leakage current (VDS=3.63V) vs. saturation current (VDS=VGS=3.3V) for NMOS (top) and PMOS (bottom).

Process parameter	*Variation*
Screen oxide temp	+/- 3°C
Gate oxide thickness	+/- 4Å
VT implant dose	+/- 3%
Lgate	+/- 10%
LDD implant dose	+/- 3%
Spacer TEOS depo temp	+/- 10°C
Spacer width	+10/-50%
SD implant dose	+/- 3%
RTP temp	+/- 10°C

Table 1 List of process parameters chosen for the DOE with associated upper/lower limits. Only spacer width limits are non symmetrical.

Lgate=10µm	Vth	Beta	Idsat
Vth	1	-0.95 (-0.66)	-0.98 (-0.90)
Beta	-0.73 (-0.66)	1	-0.99 (-0.91)
Idsat	-0.81 (-0.79)	0.98 (0.95)	1

Table 2 Correlation matrix for NMOS (left side of diagonal) and PMOS (right side of diagonal) transistors obtained from simulation. Values in bracket are from experiments over 1200 measurements points on 50 lots.

Lg=0.5µm	Vth	Beta	Idsat
Vth	1	-0.69 (-0.68)	-0.75 (-0.78)
Beta	-0.66 (-0.54)	1	-0.99 (-0.98)
Idsat	-0.80 (-0.71)	0.95 (0.93)	1

Table 3 Correlation matrix for NMOS (left side of diagonal) and PMOS (right side of diagonal) transistors obtained from simulation. Values in bracket are from experiments over 1200 measurements points on 50 lots.

Lg=0.5µm	P-Vth	P-Beta	P-Idsat
N-Vth	-0.82 (-0.45)	-0.69 (-0.51)	0.72 (0.53)
N-Beta	0.65 (0.59)	0.98 (0.89)	-0.97 (-0.85)
N-Idsat	0.77 (-0.61)	0.96 (0.88)	-0.97 (-0.88)

Table 4 Correlation matrix between NMOS and PMOS transistors for various electrical parameters obtained from simulation. Values in bracket are from experiments over 1200 measurements points on 50 lots.

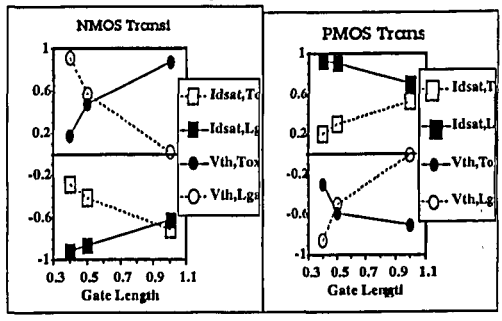

Figure 4 Correlation factor between Idsat, Vth and Tox, Lgate for NMOS (top) and PMOS (down) transistors as a function of nominal gate length.

NMOS Overlap Capa	%	PMOS Overlap Capa	%
SD_dose^2	-5.3	Spac_width*RTP_temp	6.1
Tox^2	5.3	Gate_Tox*Spac_width	-5.7
LDD_dose^2	4.5	Gate_Tox*RTP_temp	5.2
Spac_temp	4.3	Spac_temp*RTP_temp	-5
LDD_dose*Spac_width	4.1	VT_dose*Lgate	4.4
Spac_width*RTP_temp	4	SD_dose^2	-4
Lgate*Spac_temp	4		

Table 5 Signature of th influence of process parameter influence on overlap capacitance at 0V bias for NMOS and PMOS transistors. Linear, interaction and quadratic terms are presented.

Tpd of CMOS inverter	Correlation
U0 (NMOS)	+0.8451
U0 (PMOS)	+0.8048
LINT (NMOS)	-0.8835
LINT (PMOS)	-0.9010
CGDO, CGSO (NMOS)	+0.05
CGDO, CGSO (PMOS)	+0.3149

Table 6 Correlation matrix of Time Propagation Delay (Tpd) of a CMOS inverter for some BSIM3v3 SPICE parameters. Extracted values from 200 SPICE simulations of a 11stages ring oscillator.