Coupled 3D Process and Device Simulation of Advanced MOSFETs

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Abstract

A coupled fully three-dimensional process and device simulation of an advanced NMOS transistor using new 3D process simulation tools was performed. A POCKET doping resulting from large angle tilted implantation was included in the process flow. 3D effects originating from the non planar 3D mask have been analyzed. Simulation of the transfer characteristics shows a remarkable influence of 3D device and process features on electrical device behavior. A lower sensitivity to substrate bias has been observed in the 3D device compared to standard 2D simulation.

1. Introduction

The development of the next generations of integrated circuits requires not only an ongoing shrinkage of the device dimensions but also the use of more complicated device architectures in order to avoid problems resulting from parasitic effects, e.g. short and narrow channel effects or hot carrier degradation, and to ensure a sufficiently low sensitivity of the electrical device properties to fluctuations of technological parameters during device fabrication. These trends have given rise to the need to simulate the fabrication and the electrical properties of deep submicron devices no longer in two dimensions, as can be done with standard commercial simulation programs, but to take three-dimensional effects into consideration. This paper presents first results of the coupled fully three-dimensional process and device simulation of an advanced NMOS transistor using new 3D process simulation tools which are being developed in the PROMPT project.

2. 3D Process Simulation

In a POCKET type device [1], a counterdoping (p-doping in NMOS) is implanted under the gate under large tilt and rotation angles. When properly adjusted, this POCKET doping drastically reduces short channel effects which cause a threshold voltage roll-off with decreasing channel length. In the upper part of Fig. 1, the geometrical shape of a POCKET transistor with a polysilicon gate length of 0.18 μm is shown. One half of the transistor is visualized. The active area is in the right hand side of the figure with highly doped source and drain regions. The position of the gate is marked by two lines in the middle of the device.

The large angle ion implantation of boron is a critical process step for the NMOS POCKET device. This boron implantation was performed at an energy of 10 keV and a total dose of $5 \cdot 10^{13} cm^{-2}$. To form the POCKET doping below the gate, the implantation was performed with a tilt angle of 30° and rotation angles of 22°, 112°, 202° and 292°, respectively. Fig. 2 depicts the doping distribution in the NMOS POCKET transistor at the end of the process simulation. The gate material as well as the field isolation oxide shown in Fig. 1 are removed in Fig. 2 for better visualization of the dopant concentration in silicon. Fig. 2 presents a top view onto the silicon surface. Due to the strong non-planarity of the gate and the large tilt and rotation angles the doping distribution after pocket implantations exhibits strong 3D effects. These 3D effects resulting from the non-planar 3D mask are accounted for in the present simulation using a special topography projection algorithm [2].

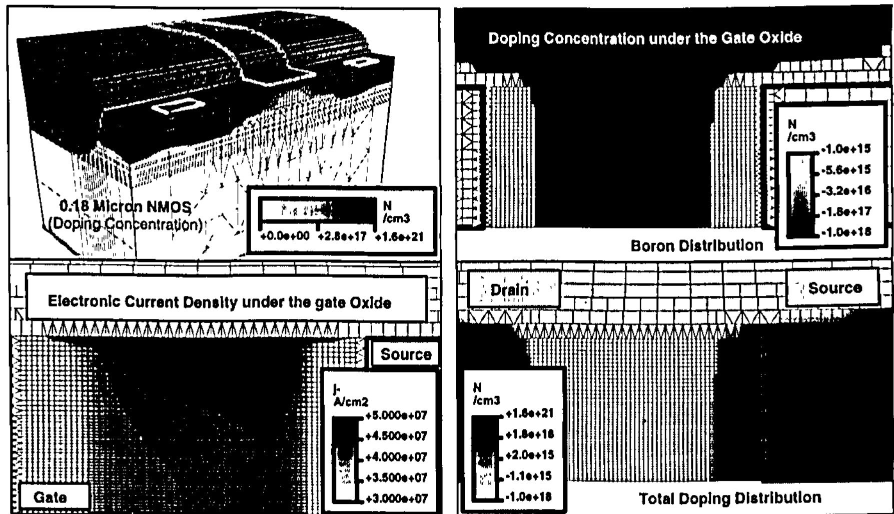

Figure 1: Three-dimensional shape and current density under the gate of an NMOS pocket type transistor with a polysilicon gate length of 0.18 μm

Figure 2: Doping distribution in the channel region after all doping and annealing steps. N-type doping: positive values; P-type doping: negative values

Especially, the POCKET doping decreases towards the lateral field oxide. This effect of the pocket implantations remains existent also in the final device as it is shown in the upper part of Fig. 2. This non-uniform distribution of the pocket doping in the lateral direction results in a variation of the effective channel length in dependence on the lateral position as well as in a variation of the local effective threshold voltage. In consequence, the current density which was simulated with the three-dimensional device simulator DESSIS increases when going from the gate axis towards the lateral field oxide.

3. Results of Device Simulation

The lower part of Fig. 1 presents the distribution of the current density under the gate when looking from the top. The current distribution is shown in the on-state of the transistor, V_G=V_D=1.8 V. The observed current distribution under the gate is strongly non-uniform. The maximum current density is at the edges of the active area adjacent to the field isolation. It exceeds the current density in the center of the gate by up to 70%. The non-uniformity extends almost over the whole width (W=0.18 μm) of the transistor. There are several physical reasons for the strong non-uniformity of the current density under the gate, especially the non-uniform doping under the gate, the Coulomb repulsion of the electrons, and the band bending at the interface silicon-to-field-oxide. Field crowding in case of overetched field oxide (corner effect) and an accompanying gate oxide thinning was excluded by the chosen form of the field oxide.

The electrical characteristics of the advanced POCKET MOS transistors obtained from the coupled fully 3D process and device simulation have been compared with those gained applying the 3D tools to a 2D geometry (infinite channel width) and the role of 3D effects have been analysed. Fig. 3 shows the transfer characteristics of the NMOS POCKET transistor simulated using a 2D and a 3D geometry, respectively. The 3D effect of the lateral current crowding results in the difference between the 2D and the 3D simulation of the transfer characteristics. In comparison, Fig. 4 shows a 2D simulation of the short channel effect.

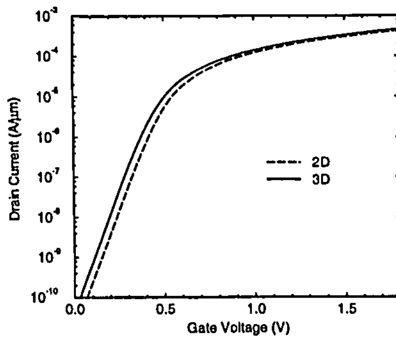

Figure 3: 3D effect in transfer characteristics of 0.18 μm NMOS POCKET transistor

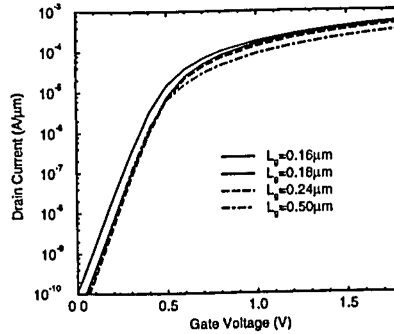

Figure 4: Short channel effect in transfer characteristics of NMOS POCKET transistors

To examine the body effect, a negative substrate voltage of 1.8 V was applied and results were compared with the non biased case. Fig. 5 shows the distribution of the current density under the gate oxide for both conditions. In contrast to Fig. 1 the drain voltage is now V_D=0.1 V, and V_G=1.8 V. The upper and lower left part of Fig.5 show the current density at silicon surface across the channel in linear scale and the right parts in the logarithmic scale. The linear plot provides an estimation of the contributions to the total current measured, while the logarithmic presentation shows the overall extension of the non-uniformity of the current density over the gate. The ratio of the current densities $j(V_{sb} = -1.8V)/j(V_{sb} = 0V)$ turns out to be 0.83 in the center of the channel and 0.95 at the channel edge, respectively. The ratio of the drain saturation currents $I_d(V_{sb} = -1.8V)/I_d(V_{sb} = 0V)$ amounts to 0.81 as shown in Fig. 6. This means that the substrate bias effect is stronger in depth than on the silicon surface.

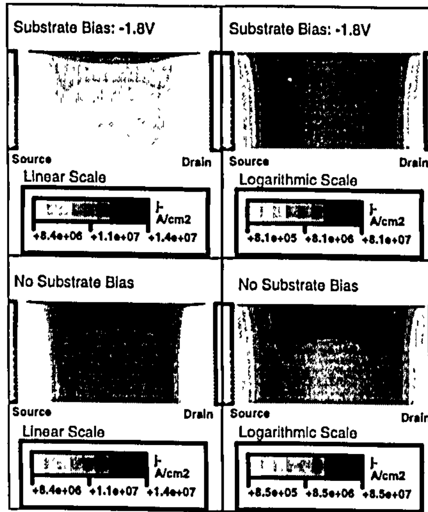

Figure 5: Comparison of current densities under the gate oxide for different substrate bias conditions

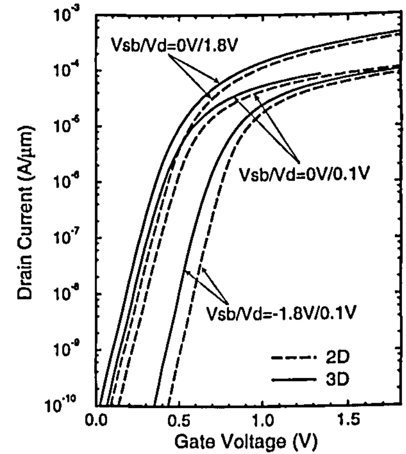

Figure 6: Comparison of transfer characteristics for different substrate bias conditions

Fig. 6 also shows that the 3D transistor exhibits a slightly smaller sensitivity to substrate bias compared to the 2D device. The corresponding body field effect coefficients are $\gamma_{3D} = 0.13$ V$^{1/2}$ and $\gamma_{2D} = 0.14$ V$^{1/2}$ for 3D and 2D simulations, respectiveley. γ was extracted using the well known relationship $\Delta V_{th} = \gamma(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f})$ and the usual estimate $2\phi_f = 0.6V$ for the bulk Fermi potential.

4. Conclusions

Electrical behavior of an advanced NMOS transistor was investigated by means of coupled fully 3D process and device simulation. 3D effects on transfer characteristics are comparable with the short channel effect simulated in 2D. Both, the doping distribution and the geometrical shape of the device, determine the strength of the 3D effects. Inhomogeneous current densities have been observed for the POCKET device which result in a smaller body effect in favour of the 3D device.

Acknowledgement

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References

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[2] J. Lorenz, K. Tietzel, A. Bourenkov, H. Ryssel, "Three-Dimensional Simulation of Ion Implantation" in: *Proc. SISPAD'96*, 1995, pp. 23-24