Accurate Layout-Based Interconnect Analysis

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Abstract

We have developed a set of simulation programs for two- and three-dimensional analysis of interconnect structures. The simulators are based on the finite element method and can be used for highly accurate capacitance extraction, resistance calculation, transient electric simulation (calculation of capacitive crosstalk and delay times), and coupled electro-thermal simulations. The layout of the interconnect structure can be imported from CIF or GDSII files, or can be created interactively with a graphical layout editor [1] which is also used to select an "area of interest" and to generate cuts for two-dimensional simulations. The geometric structure can be generated either directly from the layout by specifying constant layer thicknesses, or by a rigorous topography simulation [2]. For the creation of two-dimensional simulation grids the program Triangle [3] is used, for the three-dimensional case we perform a layer-based grid generation method [4]. As application example a polysilicon resistor pair is analyzed with the tools presented.

1. Introduction

As the performance of VLSI circuits is increasingly limited by interconnect properties, accurate three-dimensional interconnect models have become essential to chip and system design. Accurate extraction of parasitic resistances and capacitance, the calculation of crosstalk, and signal delay caused by interconnections are the most important issues. In addition, from the aspect of circuit reliability the knowledge of the current density and temperature distribution in the wiring structures is important to prevent electromigration. Experimental measurements are difficult and time-consuming and sometimes impossible at all, especially on-chip. Analytical models supplied by conventional ECAD tools prove as too inaccurate for complex geometric structures—only a fully three-dimensional simulation approach as presented in this work can supply the required accuracy.

2. Mathematical Models

For the *capacitance extraction* we use the finite element method to calculate the electric potential φ inside the insulator domain by solving the Laplace equation

$$\operatorname{div}(\varepsilon(x, y, z)\,\operatorname{grad}\varphi) = 0, \tag{1}$$

where ε denotes the permittivity tensor. Conductor surfaces are represented by Dirichlet boundary conditions. The calculation of *resistances* is performed in a similar manner by solving

$$\operatorname{div}(\gamma_E(x,y,z)\,\operatorname{grad}\varphi) = 0 \tag{2}$$

in the domains of conducting material, where γ_E is the electric conductivity.

Usually delay times or crosstalk on interconnect lines are calculated analytically based on extracted resistances and capacitances using lumped or distributed (transmission line) models. The effect of the magnetic field can be neglected in most applications. This approach is only valid for configurations where the electrical field is perpendicular to the direction of signal propagation. For general structures we can achieve more accurate results by solving the transient potential distribution function

$$\operatorname{div}(\gamma_E\,\operatorname{grad}\varphi + \varepsilon\,\operatorname{grad}\frac{\partial\varphi}{\partial t}) = 0. \tag{3}$$

For the numerical calculation of Joule self-heating effects two partial differential equations have to be solved. The first one is (2) which gives the electric potential and needs to be solved only inside domains composed of electrically conducting material. The next step is to compute the power loss density p,

$$p = \gamma_E(\operatorname{grad}\varphi)^2. \tag{4}$$

Then, the heat conduction equation has to be solved to obtain the distribution of the temperature T

$$\operatorname{div}(\gamma_T\,\operatorname{grad}T) = p - c_p\rho_m\frac{\partial T}{\partial t}. \tag{5}$$

γ_T represents the thermal conductivity, c_p the specific heat and ρ_m the mass density. Both, the electrical and thermal conductivities of certain materials depend on the temperature. Therefore, we use a linear model

$$\gamma = \gamma_0\frac{1}{1+\alpha(T-T_0)}. \tag{6}$$

γ_0 is the (electrical or thermal) conductivity at the reference temperature T_0 of 300 K, and α is a constant temperature coefficient.

3. The Program Package SAP

We have developed a program package called SAP (Smart Analysis Programs). The two main programs (SCAP: capacitance and resistance extraction and STAP: transient electric/thermal analysis) use the finite element method to solve the above partial differential equations for the calculation of the electric potential distribution, and the temperature profile. The calculations can be performed with linear and quadratic shape functions. For highly accurate results a global grid refinement algorithm is supported. For time dependent problems, the Backward-Euler and Crank-Nicholson methods have been implemented. A preconditioned conjugate gradient solver is used to solve the resulting linear systems. The calculated potential, current density, and temperature profiles can be post-processed and visualized with a program based on [5].

In this example we analyze a matched polysilicon resistor pair. Both lines are 1 μm wide, 0.5 μm thick, and have a total length of 171 μm. The polysilicon layer has a resistance of 2000 Ω□. As a preprocessing step the structure is converted from a layout file to the SAP data representation and the simulation grid is generated automatically. In the first step we extracted the resistance and capacitance with the program SCAP ($R_1 = R_2 = 3.34\ k\Omega$, $C_{1,gnd} = 19.0$ fF, $C_{2,gnd} = 19.4$ fF, $C_{1,2} = 5.0$ fF). Transient electric simulation is applied to calculate delay times and crosstalk between the resistors (Fig. 1, 2). Therefore, a voltage step of 1 V is applied on the left terminal of the first resistor, the second resistor is connected to ground and the Si-substrate has been assumed as an ideal conductor connected to ground. A delay time of 106 ps is observed until the output voltage of the first resistor reaches 90% of the input. Crosstalk occurs on the output of the second resistor, its maximum of 0.1 V is reached after 40 ps. The computed output voltages are in very good accordance with the results obtained from a calculation of a 5-stage lumped model based on the extracted R and C values. In the second transient simulation we assumed a lightly doped substrate with a resistivity of 19 Ωcm. The output voltages of the active and the grounded line (with respect to the potential of the substrate surface on the right side) are shown in Fig. 3. Note, that these results differ significantly from the previous simulation and cannot easily be obtained with a lumped or transmission line model. Thermally induced mismatch in the resistances is calculated in a coupled electro-thermal simulation run. Here, one line is loaded with a current of 3 mA, and the bottom of the Si-substrate is kept constantly at 300 K. This causes a difference of 2% in the resistances due to joule self heating.

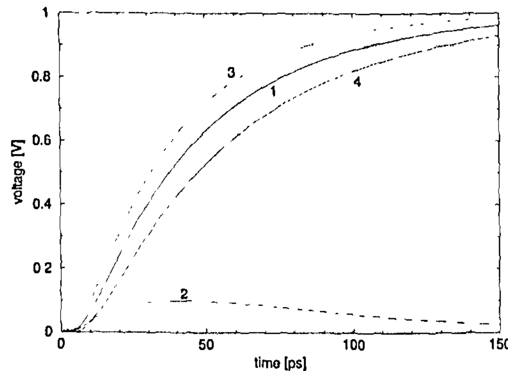

Figure 1: Output voltages of the polysilicon resistor: 1 and 2: one resistor gets a voltage step of 1 V, the other one is connected to 0 V, curve 1 shows the output voltage on the active line, delay 106 ps, 2: crosstalk on second line, maximum 0.1 V, 3: voltage step is applied on both resistors: delay 84 ps, 4: output for a straight polysilicon line with same length, delay 132 ps.

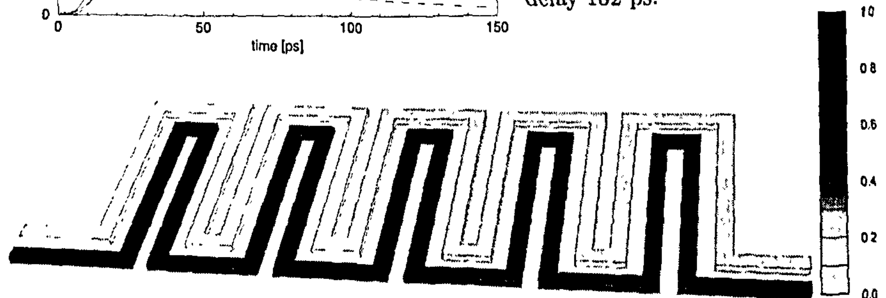

Figure 2: Potential distribution in [V] on the surface of the resistor structure 40 ps after switching the lower left terminal to 1 V.

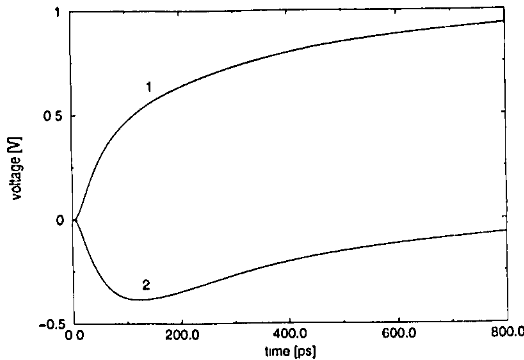

Figure 3: polysilicon resistor over lossy substrate: 1: output voltage on the active line, delay 657 ps, 2: crosstalk on second line. Note the negative crosstalk voltage which is caused by the very high resistivity of the substrate.

4. Conclusion

We introduced the interconnect analysis programs SAP and demonstrated its usefulness for highly accurate interconnect analysis with an polysilicon resistor example. The program package SAP has been tested with a large number of applications and is freely available from http://www.iue.tuwien.ac.at/software.html.

Acknowledgment

Our work is significantly supported by Sony Corporation, Atsugi, Japan, Digital Equipment Corporation, Hudson, USA, and by the ADEQUAT+ (ESPRIT 21752) Project.

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