Modeling of Temperature Dependence of a Floating Pad Structure's RF Properties

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Abstract

Temperature dependence of silicon MCM substrate RF properties is studied by modeling simple I/O structures. Both normal RF IC and high resistivity silicon substrates were processed. Lumped element equivalent circuit parameters were extracted for temperature range -60° C – +90° C.

1. Introduction

Increased demand for RF IC applications has generated interest in the use of silicon as a substrate for high frequency devices such as inductors [1,2,3]. Multi Chip Module (MCM) technology gives new opportunities to meet passive components RF application requirements. In this work we have used integrated passive process on low and high resistivity silicon substrates. Compared with GaAs techniques, a major concern in silicon substrate technology is the power lost to substrate at high frequencies. Interference issues such as inductor induced substrate noise [4] set requirements also to signal isolation.
Modeling of silicon substrate properties is required to improve RF designs. In this paper the behaviour of high impedance pad structures for RF applications is modeled and characterised in the temperature range -60° C to 90° C. This model can then be used in modeling the pad structure in RF designs. The model was tested in the frequency range 45 MHz to 18 GHz and in the temperature range -60° C to +120° C. The limitations of the measurement system in such extreme conditions are discussed.

2. Experimental set-up

The test structure was a pad/ground structure as shown in Fig.1. The diameter of the signal pad was 75 µm and distances between pads was 1.2 mm. Wafers were fabricated using an experimental silicon based MCM process. In this process substrate was floating i.e. there was no substrate contacts on front or backside. Insulator between the

metallisation and the silicon substrate was 3.4 μm thick silicon dioxide. Metal layer was 8 μm thick electroplated gold.

Two different substrates were used in tests. First substrate was typical RF IC starting wafer. This p-type wafer had resistivity ≈ 20 Ω-cm. Second substrate was n-type detector grade silicon wafer – resistivity ≈ 10 kΩ-cm.

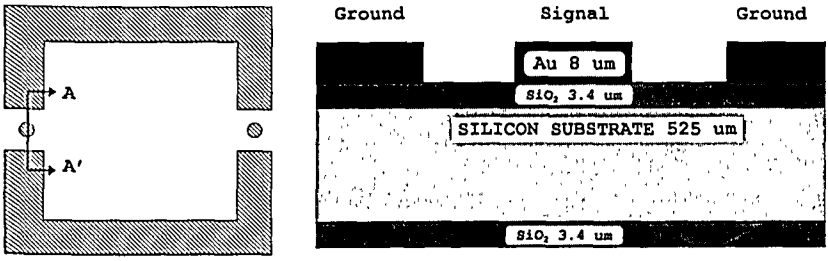

Figure 1: Test structure layout and cross section.

The test structures were measured with HP8510C network analyser and Summit 12000 probe station. Probe station was equipped with temperature controlled chuck. SOLT calibration was done with calibration substrate attached to the probe station near the wafer chuck. Calibration was performed before each measurement in different temperatures. Measurements were made from 60° C to +120° C in 30° C increments.

Preliminary measurements showed that S-parameter values measured at 120° C were not reproducible. Reason for this was equipment calibration problem. At high temperatures there was a large temperature difference between the calibration substrate and the wafer. Also probe tip impedance had a strong temperature dependence at temperatures above 100° C. The solution would be separate heating of the calibration substrate to the chuck temperature and correction for probe impedance change caused by heating of probe tips and transmission lines.

3. Pad model and measurement results

A simple equivalent circuit [2,5] is used for pad modeling, Fig.2. C_{PAD1} represents oxide capacitance, G_{SUB1} and G_{SUB2} represent silicon conductances and C_{SUB1} and C_{SUB2} represent silicon capacitances. In parameter extraction C_{PAD1} is calculated from known pad dimensions and oxide thickness. As C_{SUB1} and G_{SUB1} are small compared with C_{SUB2} and G_{SUB2}, C_{SUB2} and G_{SUB2} can be calculated from the measured input impedance at constant frequency.

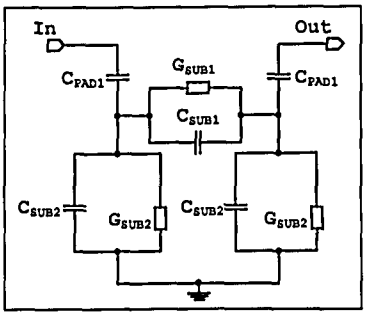

Figure 2: Pad model

$$Y_{SUB2} = \left(Z_{IN} - \frac{1}{j\omega C_{PAD1}} \right)^{-1},$$

$$C_{SUB2} = \mathrm{Im}\left\{ Y_{SUB2} / \omega \right\},\ G_{SUB2} = \mathrm{Re}\left\{ Y_{SUB2} \right\}$$

Better model fit was achieved when calculation was done at constant input capacitance value. Frequency for above calculations was selected so that $C_{IN} \approx \frac{1}{2} C_{PAD1}$.

Calculated model parameters for 20 Ω-cm wafer are summarised in Table 1. Fitting of simulated and measured input capacitance and conductance is shown in Fig.3. The model for input impedance can be used from DC to 10 GHz. Model parameter G_{SUB2} has a negative temperature coefficient and parameter C_{SUB2} is independent of temperature (Fig.4). This is consistent with Groves et al [6] and 2D finite element AC simulation.

Table 1: Model parameters vs. temperature

T °C	C_{PAD1} fF	C_{SUB2} fF	G_{SUB2} mS	C_{SUB1} fF	G_{SUB1} uS
-60	41.65	16.24	1.10	↑	↑
-30	41.65	16.30	0.85	↑	↑
0	41.65	16.28	0.62	↑	↑
30	41.65	16.20	0.49	1.43	72
60	41.65	16.47	0.42	↓	↓
90	41.65	17.40	0.39	↓	↓

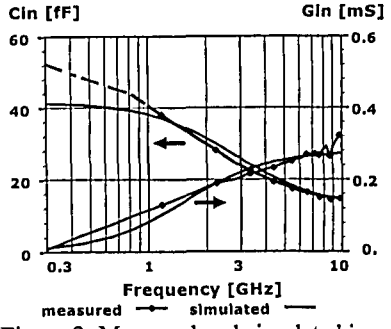

Figure 3: Measured and simulated input capacitance and conductance at 30° C.

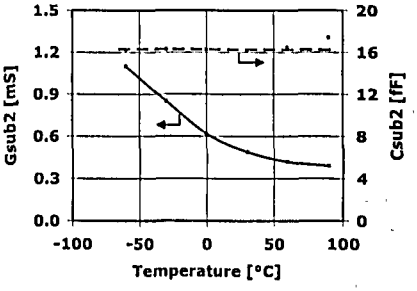

Figure 4: Substrate conductance and capacitance versus temperature.

At high frequencies capacitance C_{PAD1} presents a low impedance path to the signal. The temperature dependence of G_{SUB2} affects total input capacitance C_{IN} of the pad structure Fig.5. The frequency at which C_{IN} reduces to half of C_{PAD1} is presented in Fig.6.

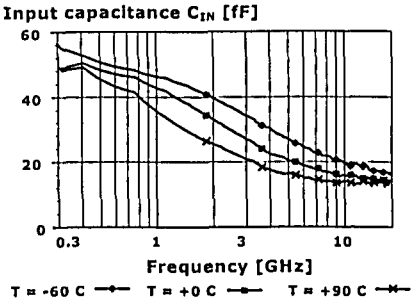

Figure 5: Input capacitance versus frequency.

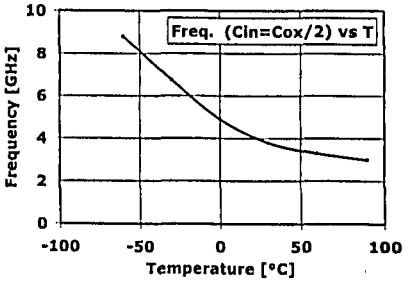

Figure 6: Constant capacitance frequency versus temperature

Fitting of the phase and magnitude of S_{21} (signal leakage) at high frequency is used for G_{SUB1} and C_{SUB1} determination. The fit between the simulation and measurement of S_{21} is relatively poor. Magnitude of S_{21} is not temperature dependent.

For high resistivity (10 kΩ-cm) wafers parameter G_{SUB2} is two to three orders of magnitude smaller than for IC wafers. So at high frequencies input impedance of pad structure is dominated by substrate capacitance C_{SUB2}. S_{11} is near unity because of high impedance level. Small measurement errors in S_{11} cause large relative errors in calculated impedance.

4. Conclusions

Pad test structures on two different substrate materials were processed and measured. The problems encountered with high resistivity material was discussed briefly above. Structures on RF IC wafers were selected for detailed RF modeling. A simple lumped element equivalent circuit was used. Circuit parameters were extracted directly from measured S-parameters.

Structures were measured in the temperature range -60° C – +120° C. Problems were encountered at the highest temperature and the data was dropped from the analysis. Parameter G_{SUB2}, that models losses in silicon substrate, has a negative temperature coefficient, and other model parameters do not depend on temperature. 2D finite element AC simulation gives same temperature dependence. Isolation between the input and output pads is independent of temperature.

Acknowledgement

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