Layout-Based 3D Solid Modeling of IC Structures and Interconnects Including Electrical Parameter Extraction

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Abstract

A suite of software tools have been developed to model IC structures including interconnects based on layout design and processing information. The modeling capabilities include 3D rendering of solid objects, surface meshing, electrical parameter (mainly capacitance) extraction for arbitrarily shaped objects. This software ensemble provides a direct link between design parameters and electrical performance. Analysis of a four transistor SRAM cell is used as an example.

1. Introduction

Accurate analysis of IC devices and interconnects in the deep submicron regime increasingly depends on the precise geometry of structures. Moreover, timely technology development requires the prediction of circuit performance based directly on the design data. The current commercial tools often lack the ability to model and simulate IC structures with complex 3D geometry. This paper describes 3D simulation capabilities which directly link the impact of layout and processing and the electrical characteristics of complex IC structures and especially interconnects. Two distinct features of the system are: (1) 3D solid representation that can be updated automatically based on the design flow of layout and process specification; (2) robust and efficient meshing capabilities which make possible the electrical parameter extraction from realistic structures.

2. System Configuration

The 3D modeling approach consists of three major components: geometry modeler, mesh generator, and electrical parameter extraction. As is shown in Fig.1, the inputs are layout design (in GDS II format) and process specification. The ACIS (from Spatial Technology) geometry modeler results are shown here, but other geometry modeling tools are also being used. The geometry can be viewed and manipulated using either commercial tools (i.e., AVS) or public domain (VRML - Virtual Reality Modeling Language) browsers. For the extraction of electrical parameters, 3D objects must be meshed. Mesh generation uses the level-set algorithm being developed at Stanford[1]. Surface meshing of the structures, in support of tools that employ a boundary element method (i.e., FASTCAP), is then applied for electrical extraction.

3. Layout-Based 3D Solid Modeling

Layout (GDSII files) and process (e.g., layer thickness or simulated bird's beak shape) information are incorporated using a custom C program. The control flow follows the actual processing sequence such as deposition and etching layer-by-layer. The geometry modeler is then used to generate the 3D structures [2]. The description file for geometry is then converted to geometry files, readable for visualization. This object can be viewed from different angles or sliced by arbitrary cut-planes resulting in 2D cross sections or 3D slabs. The resulting geometric model can be represented in VRML; the device can be studied layer by layer or as a full image using simple browser across the internet. The structures are both complex and realistic as shown in Fig.2 – for remote access see http://www-tcad.stanford.edu/tcad/SRAM/.

4. Level-Set Method for Surface Meshing of Complex Geometry

The mesh obtained by simply triangulating the geometric model from a solid modeler limits the accuracy of the subsequent simulation. The level-set method [1] is adapted to generate a surface mesh of these 3D structures. Octree grid and boundary surfaces are generated instead of quadtree grid and boundary curves. Surface polygons from the solid modeler are triangulated into a coarse mesh. Octants containing the geometric model are then subdivided, recursively until a predefined refinement criteria is satisfied. The distance at each grid point is assigned a sign (+/- according to level-set 0). Octants intersecting the surface are segmented into triangles according to these signed distances. Local connectivity is extracted from the octree grid.

Details of a level set refinement for the word line are demonstrated in Fig.3 and Fig.4. Fig.3 shows a 2D cross section for a 6 level-refined octree mesh as well as the contour values of distances; Fig.4 shows the 3D iso-surface at zero distance along with volume octree mesh. As a result of 3D surface meshes, 1252 triangles are generated for word line and 5022 triangles for the substrate. A complete surface mesh includes a substrate (grey), the polysilicon layer (purple), and the two metal layers (blue and skyblue) shown in Fig.5, where the polysilicon layer includes a word line, a ground line and gates – for remote access see http://www-tcad.stanford.edu/tcad/SRAM/.

5. Capacitance Extraction for a Four-Transistor (4T) SRAM Cell

To analyze realistic structures, FASTCAP [3] is used owing to its ability to handle complicated surface topology. The boundary-element based algorithm for computing the capacitance is based on a generalized conjugate residual iterative technique.

The 4T SRAM's word line capacitance is first extracted. For a cell size of $5 \times 7.25\mu m^2$ (feature size is $0.6\mu m$), the resulting capacitance values are shown in Fig. 6. For the two bitlines, capacitance between one bitline and the substrate is 1.75 fF while capacitance between the other bitline and the substrate is 1.77 fF. The capacitance between two bitlines is 1.07 fF. One can simulate the wordline, bitlines and the substrate as a whole structure. The results are shown in Table 1.

6. Discussion

A technology-based interconnect modeling approach is presented. Capabilities of this software allow more physically accurate parameter extraction for IC circuits and interconnects. Extracted electrical parameters provides essential design information.

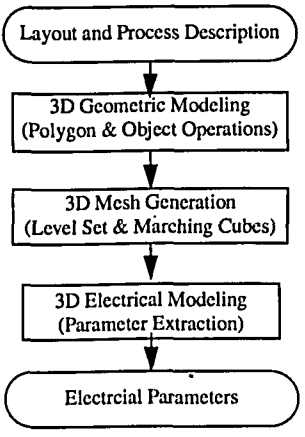

Fig.1 System flow chart

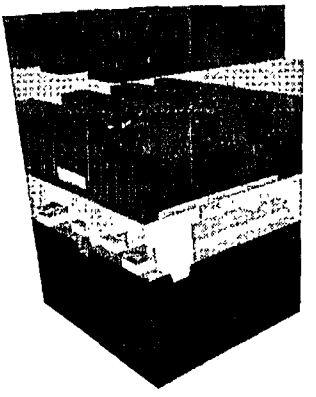

Fig.2 3D SRAM rendering with transparent layers

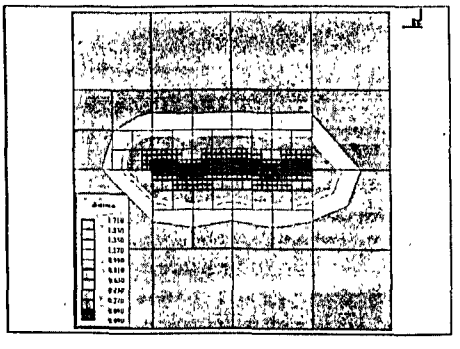

Fig.3 Distance contour and octree mesh sections for word line

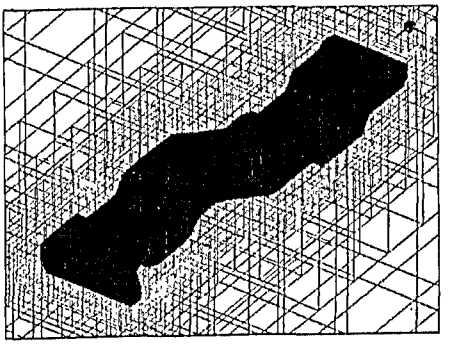

Fig.4 Iso-surface and octree mesh for word line

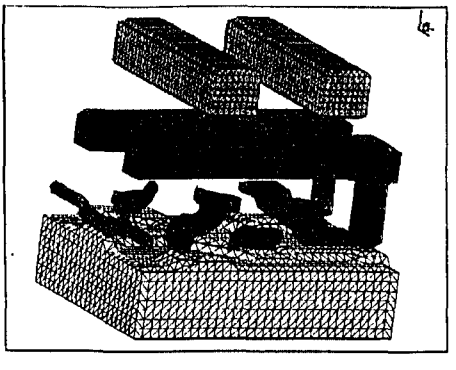

Fig.5 Silicon substrate, polysilicon layer, first and second metal layers in surface mesh

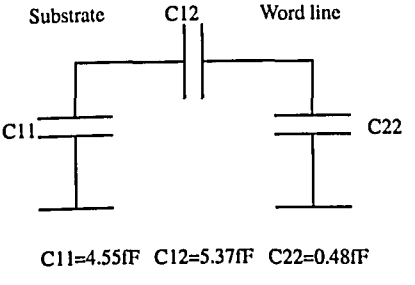

Fig.6 Capacitance for a single word line and substrate

	substrate	*wordline*	*bitline1*	*bitline2*
substrate	11.4fF	4.96fF	1.42fF	1.41fF
wordline	-	6.14fF	0.48fF	0.52fF
bitline1	-	-	3.92fF	1.04fF
bitline2	-	-	-	3.97fF

Table 1: Capacitance among the wordline, bitlines and substrate

Benchmark calculations of a simplified geometry model were also performed on a commercial simulator (Raphael from Avant!). There are differences between these results, owing to nonidentical geometries. In addition, packaging parasitics (e.g. bonding wires) can also be modeled based on the same geometry information. For example, SEM photos can be used to extract geometry information. Inductance analysis tools such as FASTHENRY can in turn be used to extract package inductance [4].

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