Exponential Expansion for Rapid and Accurate Extraction of Interconnect Capacitance

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Abstract

We report a new approach for efficient computation of capacitance in multi-conductor systems embedded in homogeneous or multiple dielectric media. The technique employs exponential expansion of the Green's function $\frac{1}{r}$ for evaluation of the three-dimensional potential and its gradient, enabling rapid and accurate extraction of interconnect capacitance in VLSI and large-area amorphous silicon electronics. Additionally, it can be used for analysis of electrostatic interaction in micro-electro-mechanical systems (MEMS).

1. Introduction

The capacitance is calculated from the distribution of charge density. Here, given a conductor system $S_1, S_2, \ldots, S_n$ with the applied voltages $V_1, V_2, \ldots, V_n$, we need to determine the charge density σ on these conductors' surfaces. The potential $\phi(x)$ due to a charge density σ on a surface $S = S_c \cup S_d$, where S_c and S_d denote conductor surfaces and interfaces between dielectric layers, is given by:

$$\phi(x) = \int_S G(x,y)\sigma(y)dy, \tag{1}$$

where G(x,y) is the associated Green's function $\frac{1}{r}$:

$$G(x,y) = \frac{1}{4\pi\|x-y\|}. \tag{2}$$

The model equations for the charge density in the multiple dielectric multi-conductor system are [1]

$$\begin{cases} \phi(X) & = V_i, \quad X \in S_i \\ \sigma(X) + 2\frac{\epsilon^- - \epsilon^+}{\epsilon^- + \epsilon^+}\nabla\phi(X)\cdot n & = 0, \quad X \in S_d. \end{cases} \tag{3}$$

The first equation signifies the equipotential on the surface of each conductor. The second signifies the flux continuity across the interface of two dielectric layers of dielectric constants ϵ^+ and ϵ^-. The overall accuracy and computational performance in solving the above model equations lies in the evaluation of the potential $\phi(x)$ and its gradient $\nabla\phi(x)$ at all N points of interest. Central to the computation lies in the representation and subsequent operations of the Green's function.

A popular method for computation of capacitance in VLSI interconnects and MEMS [2]

employs the Fast Multipole Algorithm (FMA) [3], which relies on multipole expansion (MP) of spherical harmonics for the Green's function $\frac{1}{r}$. As a hierarchical algorithm, the FMA relies on creating a tree-like hierarchy of cubes to facilitate charge clustering and declustering operations performed by translations. With the FMA, to evaluate the potential with accuracy of $O(\frac{1}{2^p})$, where p is the order of the multipole expansion, the computational time is of $O(p^3 N)$ and the associated memory requirement is of $O(p^2 N)$. However, this memory requirement of $O(p^2 N)$ can impose a severe constraint when a large N and a high p is expected. The former may be required to resolve geometrically complex structures such as a-Si TFTs and the latter is needed for accurate evaluation of the electric field at the interfaces as well as to ensure that the error in the computed charge density is not due to the approximation of the potential and its gradient. These concerns led us to the development of the exponential expansion (EE) based method. The EE method was first briefly reported in [4] and detailed in [5].

2. Exponential expansion

The approach is based on an exponential integral representation of Green's function:

$$\frac{1}{r} = \frac{1}{\sqrt{x^2 + y^2 + z^2}} = \int_0^\infty e^{-\lambda z} J_0(\sqrt{x^2 + y^2}\lambda)d\lambda, (z > 0) \tag{4}$$

which is the Laplace transform of Bessel function J_0 of the first kind with order 0. An approximation of (4) using Gauss quadratures yields:

$$\frac{1}{r} \approx \sum_{l=1}^{S_{app}} \beta_l E_l(x,y,z), \forall (x,y,z) \in D, \tag{5}$$

where the β_i's are constants, S_{app} denotes the size of the approximation, D is the domain of interest, and the $E_l(x,y,z)$'s are functions on D that are independent of each other and have the following property (see Fig. 1):

$$E_l(x_1 + x_2, y_1 + y_2, z_1 + z_2) = E_l(x_1,y_1,z_1)E_l(x_2,y_2,z_2). \tag{6}$$
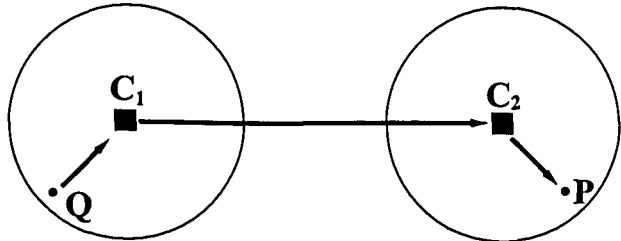

Figure 1: A translation from Q to P through centres C_1 and C_2: $E_l(QP) = E_l(QC_1) \times E_l(C_1C_2) \times E_l(C_2P)$.

The parameter values in (5) can be generated using the randomized algorithm reported in [6]. The approximation of $\frac{1}{r}$ is performed through the evaluation of the $E_l(x,y,z)$'s as a sequence of translations (see Fig. 2): clustering (Q2S, S2S), shifting

(S2T), and declustering(T2T and T2P). Each E_l can be evaluated in parallel or in sequence. For the latter, one memory unit can be used for all E_l's, thus the memory requirement is independent of the designed degree of accuracy. For the former, different parallelisms are available for remotely distributed networks and close coupled parallel systems. The features of the EE method are summarized in Table 1. All the translations have the same simple structures (see Fig. 1). There is distinct independence between the translations and the underlying expansion (4), thus allowing the overall accuracy and computational performance to be controlled externally.
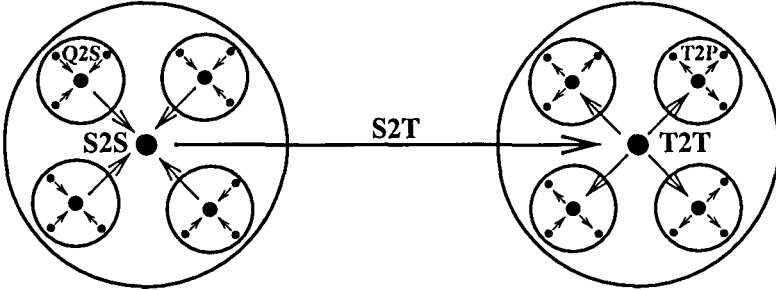

Figure 2: Translations with EE in a hierarchical structure

Features	Description	Reference
Simplicity	in translations	Figs. 1 and 2
Accuracy	10^{-3}–10^{-14}	Fig. 3
Time	$O(S_{app}N)$	Fig. 4
Memory	$O(N)$	cf. $O(p^2N)$ in FMA
Parallel processing	E_l and translations	cf. only translations in FMA

Table 1. Features of the EE method.

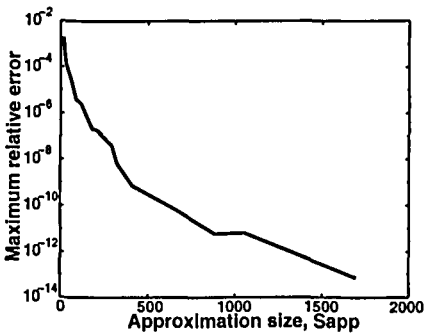
Figure 3: Maximum relative error in computed potential for a sample of size 10,000 as function of the approximation size S_{app}.
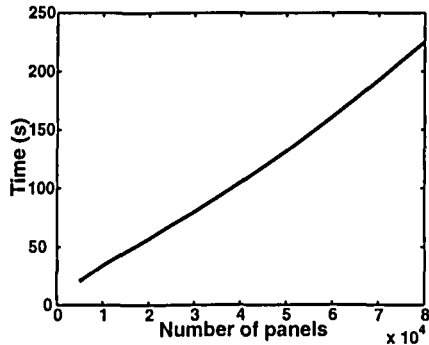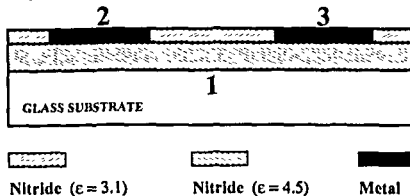
Figure 4: Computational time as function of number of panels. Approximation size $S_{app} = 31$. Maximum relative error $< 10^{-3}$.

3. Capacitance

Results of capacitance computed using the EE method are shown in Table 2 for a simple interconnect structure typical to an a-Si based imaging array (Fig. 5). Here (1,2,3) correspond to metallization interconnect layers. In comparison to the VLSI interconnect problem, the added difficulties here are the presence of the glass substrate (which constitutes a floating potential) and the small thickness of thin film layers relative to other physical dimensions (the aspect ratio is of order 10^{-3}). The conditions of the simulation are as follows. The panel number N is 319,372 and the computational accuracy (relative error) on the potential and electric field is 10^{-7} and 10^{-5}, respectively. Here, the approximation size in the exponential expansion is $S_{app} = 116$.

Figure 5: Schematic cross-section illustrating a typical interconnect arrangement in large-area imaging arrays.

	(1)	(2)	(3)
(1)	1.631×10^2	-8.121×10^1	-8.121×10^1
(2)	-8.121×10^1	8.358×10^1	-6.986×10^{-1}
(3)	-8.121×10^1	-6.986×10^{-1}	8.358×10^1

Table 2: Capacitances (fF) of the interconnect structure shown in Fig. 5.

4. Conclusion

The EE method provides a computationally efficient alternative to MP methods for evaluation of the three-dimensional potential and its gradient, enabling rapid and accurate extraction of interconnect capacitance in large-area electronics. With the memory requirement independent of the desired degree of accuracy and with various forms of parallelism available, the EE method makes possible large-scale simulations involving panel count in the range of a few hundred thousand to several million.

References

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