Single Electron Memory Device Simulations

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The final target of single-electron memory (SEM) device is to realise high-density and fast non-volatile RAM (random access memory). In this talk the simulations are discussed based on experiments and achievable nano-technologies.

1. Influence of offset charge

The characteristics of single-electron tunnelling (SET) devices are strongly affected by offset charge due to the unwanted traps of electron near the device. If trap density is high, offset-charge free circuitry should be considered. However, this approach requires more elements and results in inferior performance. The influence of offset charge on the characteristics of multiple tunnel junction (MTJ) was calculated by combining capacitor simulator and SET simulator. It is found that Coulomb blockade could not be broken if trap density is low. For example, if trap density is $10^{10}cm^{-2}$ which is a typical value of silicon interface state density, offset charge problem can be overcome by MTJ if the island size is less than 30nm.

2. Basic characteristics

The basic characteristics of single-electron memory have been studied using SET simulator including co-tunnelling effects. The conditions to obtain 10 years retention time and 1 nsec write time were examined. In metal system, 0.1 nm island diameter is required for the room temperature operation. In semiconductor system there are several possibilities to achieve room temperature operation in larger islands.

3. SET/MOS combined memory cell

To read the existence or absence of small number of electrons, gain cell approach is necessary where the stored information is amplified by active transistor in each memory cell. One of the approaches is to use conventional MOS transistor to sense the stored information since MOS transistor has large drivability whereas SET has long retention ability. SET/CMOS hybrid simulatior has been developed based on the combination of SET simulator and SPICE circuit simulator and the optimum conditions of SET/MOS memory cell were obtained.

4. Cell array

The selected read and write of single-electron memory cell array are simulated and the stable operation is demonstrated in wide parameter range.