Rigorous Capacitance Simulation of DRAM Cells

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Abstract

As dynamic RAM cell size is being scaled down, the storage capacitor design becomes more difficult because its capacitance cannot scale as much. The solutions are leading to complex structures which require an accurate description of the fabrication process, making technology CAD (TCAD) simulations necessary. We introduce a set of layout-driven TCAD tools to perform capacitance extraction of three-dimensional structures created by rigorous topographic simulation, suitable in the development of new cell configurations. Simulation results are also given and compared with measured data.

1. Introduction

Obtaining a sufficient large value of storage capacitance in a reduced cell area is becoming harder and harder and causing a more complicated capacitance electrode. Even using dielectric films with higher permitivity (e.g. Ta_2O_5 and BST) the capacitor structures are highly non-planar and their capacitances can be calculated only with numerical simulation. Realistic solid modeling of these cells requires also accurate topography simulators. We present an integrated environment where all steps towards maximum precision are considered, namely the use of accurate topography simulation [1] (with optional lithography analysis) and a state of the art finite-element solver [2] (see Fig. 1). The numerical approaches when compared with stochastic [3] or analytical ones, require more time and computer resources. Yet, for problems with the dimensions of a DRAM cell those penalties are not too severe, especially if we take in consideration the gain in accuracy obtained.

To understand the coupling between the process parameters and the electrical performance of the DRAM, the tools link the ECAD and TCAD environments as shown in Fig. 1. The result is a circuit level SPICE compatible model, where the nodes are annotated according to the names specified in the layout file that can be imported from CIF or GDS2 formats. The process recipe contains all information necessary for the topography simulators.

2. Simulation Methods

As DRAM cells are strongly non-planar structures, simulators that generate the topography directly from layout can not be used. We use the simulator etch3d [1] for

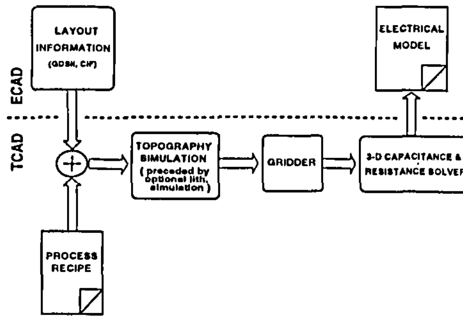

Figure 1: Data flow of proposed tools.

topography simulation. It applies methods based on morphological operations derived from image processing, which are performed on a cellular material structure where the formation of unphysical surface loops is completely avoided [1]. In the cellular format materials are represented as a three-dimensional array of cubic cells, where each byte maps to a unique material (and zero its absence). Due to the nature of this data format there are problems in the linkage with the finite element based capacitance and resistance/thermal simulators that require a tetrahedral grid.

The preprocessor laygrid [2] was written to generate three-dimensional (tetrahedral) grids compatible with the used finite-element simulators. The structures are formed and gridded by stacking planar layers (that are associated with some thickness). Each layer is made of faces with contacts (specifying net names and external voltage/current conditions) and material references.

Although laygrid is based on a layered description, it can be applied to grid the structures created by the topography simulator. The basic concept is to sample planes in the z-direction of the array of cubic cells. Each plane can be viewed then as a bitmap image with pixel colors equal to the material indexes. If an edge-detection algorithm is applied, polygonal faces defining material boundaries are found and can be used to build one layer of the structure. A new layer is inserted if the difference between the actual image and the last inserted is larger than an error criterion. An advantage of this gridding procedure is its simplicity and robustness.

The three-dimensional gridded structure is then input to SCAP [2] to extract the capacitor values. It uses the energy method for high numerical accuracy and the solver is based on optimized finite-element techniques.

3. DRAM Simulations

The vertical stacked capacitor is one of the most commonly used electrode types in modern DRAMs. We simulated this structure as described in [4]. The several stages in the process flow of the capacitor are shown in Fig. 2. Its diameter is 1 μm, the height 800 nm and the wall thickness of the storage node is adjusted to 80 nm.

Fig. 3-left shows a SEM after the storage plate formation – step (d) – and the grid of the simulated structure is presented in Fig. 3-right (only the elements of material POLY1 are shown). The total structure has 1 million elements, the extracted value is 26.1 fF and matches well with the measured value of 23.3 fF. Although the displayed structure exhibits almost cylindric symmetry a full three-dimensional simulation was performed. The total run time of the topography simulation is 27 minutes in a DEC 3000/400 workstation.

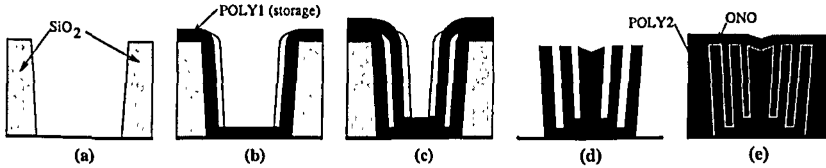

Figure 2: Process flow of the vertical stacked capacitor.

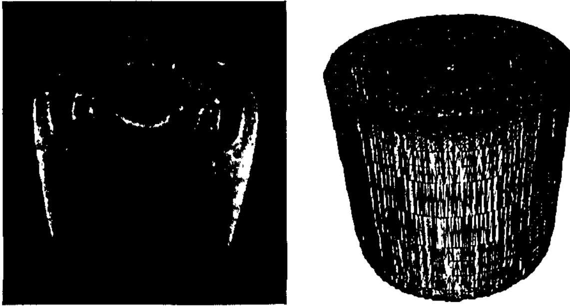

Figure 3: Vertical stacked capacitor: Left – SEM photograph of the storage plate. Right – Grid of the simulated structure (only the material POLY1 is presented).

Next we present results for a variation of the stacked trench cell as in [5]. To avoid sharp edges at the corners of the trench, an oxidation and stripping step was performed before the formation of the 100 nm dielectric layer. Since the bit-line capacitance is a very important parameter, we investigate the error introduced by assuming a perfect planarization of this line. For this situation the grid used is shown in Fig. 4-left. The very dense grid in the trench capacitor is necessary because the thin dielectric layer must be resolved. Following we performed a topography simulation for the complete cell, which solid model is depicted in Fig. 4-right. The extracted capacitances for both cases and the measured values are presented in Table 1. From these we conclude that simple models for the bit-line strongly underestimate its parasitic capacitance, confirming the need for topography simulation. The small difference still existing to the measured value is due to the neglection of the capacitance between adjacent bit-lines and due to variations in the process parameters. The number of nodes was 10^5 and $2 \cdot 10^5$ for the first and second case, respectively, corresponding to run times of 10 and 21 minutes on a DEC 3000/400 workstation, obeying an almost linear dependence.

These tools can also be used to optimize the layout design of other parts of the DRAMs, as parasitic capacitors are associated with circuit performance. By example, the reduction of the capacitive imbalance in the sense amplifier lines is very important to its optimal operation, and in general smaller parasitic capacitors mean faster electronics and less power consumption (namely in the I/O buffers).

Table 1: Results of the trench DRAM cell simulation (values are in fF)

	C_{trench}	C_{bit_line}	C_{word_line}	$C_{bit_line,word_line}$	C_{bit_line}/C_{trench} (128 cells)
Planar Metal	40.1	1.04	2.22	0.34	2.9
Acc. Metal	40.1	1.72	3.35	0.42	5.5
Experiment	38.2	1.88	-	-	6.3

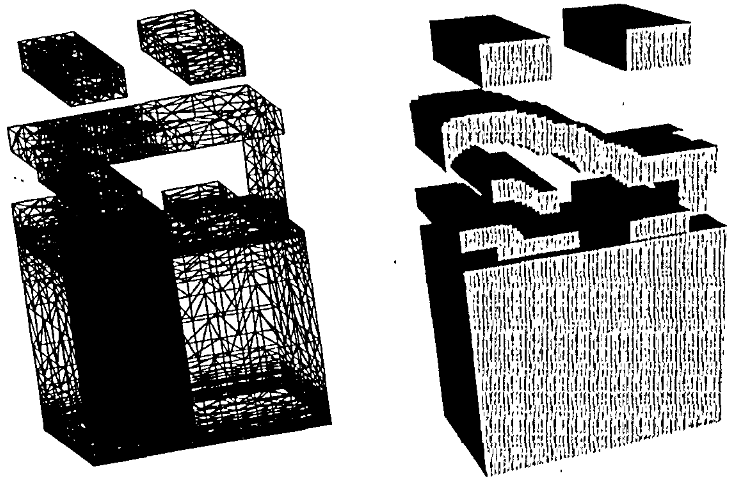

Figure 4: Trench DRAM cell: Left – Grid assuming planar interconnect lines. Right – Solid model after topography simulation of interconnect lines.

4. Conclusion

We presented an integrated environment capable of three-dimensional capacitance extraction over structures created with accurate topography simulators. Its application to common DRAM cell types give results very close to the measured data, which demonstrates the accuracy and generality of the proposed tools.

Acknowledgments

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