Characterisation of the Corner Effect by composed 2D Device Simulations

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Abstract

In scaled down MOSFET's isolated by trenches the threshold voltage is dominated by the corner effect. In this work a method is presented which allows to compose the gate characteristic of corner devices from 2D simulations. The composed results are compared with 3D simulations. The method has been applied successfully for gate lengths and gate widths down to .4μm and for bulk voltages down to -3.3V (nMOSFET). In cases where no shoulder is observed in the gate characteristic the presence of the corner effect can be identified by the comparison of 2D and composed results without expansive 3D simulations.

1. Introduction

Usually scaled down MOSFET's are isolated by trenches. Fringing gate fields enhance the carrier inversion within the silicon corner at the isolation edge. Characterisation of these corner devices requires 3D device simulations which are still expensive. On the other hand the corner effect dominates basic device charecteristics especially the threshold voltage. We present a method which allows to compose the gate characteristic of corner devices from 2D simulations for large variations of device dimensions and of the bulk voltage. The results are compared with 3D simulations.

2. Method

Starting from the drift diffusion approach (equ.(1) in tab.1) the method is based on the following idea: The electron velocity *vel* can be determined by a 2D simulation in the plane in length direction of the device (l-cut, Fig.1, Fig.2a). *vel* is calculated from the drain current $I_{dc,l-cut}$ normalized to the sum *snl* of the electrons n in the l-cut (equ.(3) in tab.1). The sum *snw* of the electrons n contributing to the drain current I_{dc} can be determined by a 2D simulation in the plane in width direction (w-cut, Fig.1, Fig.2b). *snl* is an 1D integration (equ.(2)) into the depth of the channel at the center point of the device where l-cut and w-cut cross each other (Fig.1, dashed lines in fig.2a). *snw* is a 2D integration (equ.(4)) over the complete plane of the w-cut (fig.2b) regarding for enhanced carrier inversion due to fringing gate fields. The drain current I_{dc} for the composed 2*2D simulation results from equ.(5). The simulations are performed with MEDICI and DAVINCI /1/. Both tools provide

statements yielding values for *snl* and *snw*. Fig.3a shows corresponding values as a function of the gate voltage V_{gc}. Fig.3b shows the gate characteristics resulting from the full 3D simulation (structure in Fig.1), from the 2D simulation in the l-cut (structure in Fig.2a) and from composed 2*2D simulations. The 3D structure of the nMOSFET has been calibrated to measured gate characteristics by 3D simulations.

$$j_n = \mu_n n \nabla E_{fn} = v_n n \quad (1)$$

$$snl = \int_D n \, \partial d \quad (2)$$

$$vel = I_{dc,l-cut}/snl \quad (3)$$

$$snw = \int_{W/2} \int_D n \, \partial d \, \partial w \quad (4)$$

$$I_{dc} = vel \; snw \quad (5)$$

j_n: current density,
n: density, μ_n: mobility,
E_{fn}: quasi Fermi level, v_n: velocity for electrons respectively.

w: width, d: depth,
W: width and D: depth of the Device.

3. Assumptions:

The method is valid under two assumptions: 1.) The electron velocity must be constant along the width direction which can be shown by 3D simulations. 2.) The gradual channel approximation must be fulfiled. Thus the method is restricted to small drain voltages V_{dc}. If drain fields do not contribute to the carrier inversion then the quasi Fermi level E_{fn} in the w-cut can be set to the source potential (.0V in all cases). This is necessary at non zero bulk voltages. The value of E_{fn} in the channel region is given by the voltage at the source/drain electrodes which are not included in the w-cut.

4. Corrections

Depending on device dimensions and voltage conditions different corrections must be performed. No information from the 3D simulations is necessary. The two main corrections are:

1.) A correction is necessary if *vel* increases at V_{gc} at which the electron density reaches the doping level in the channel (between V_{gc}^{1l} and V_{gc}^{2l} in fig.3a). In the corner of the 3D device electron density reaches the doping level at smaller V_{gc} (between V_{gc}^{1w} and V_{gc}^{2w}). The composed $I_{dc}(V_{gc})$ curve can be improved by a shift (arrow in fig.3a) of the $vel(V_{gc})$-curve (with further modifications). The result is shown in fig.3c.

2.) *snl* in the l-cut and the integrated electron density *snw.cp* in the w-cut at the center point of the device (dashed line in fig.2b) must be equal. At small gate length L_g or small gate width W_g and at non zero bulk voltages *snl* and *snw.cp* can have different values. The reason is that in small devices the bulk potential does not reach the channel area at the same extent as in devices with larger dimensions (reduced body effect). A w-cut e.g. includes no information about L_g and thus the reduced body effect occuring in the l-cut is not regarded in the corresponding w-cut. This can be corrected by reducing the bulk voltage in the w-cut ($V_{bc,eff}$) in a way that *snl* and *snw.cp* are equal. Then 3D and 2*2D results show good agreement (fig.4). If a reduced body effect occurs in the w-cut (due to small W_g), then V_{bc} in the l-cut must be modified correspondingly. If a reduced body effect occurs in the l-cut and in w-cut, the method cannot be applied.

5. Results and Conclusion

This method has been applied for .4≤ W_g ≤10.μm, .4≤ L_g ≤5.μm and .0≤ V_{bc} ≤-3.3V. In all cases the method was successful: good agreement between 3D and 2*2D is achieved with no additional fitting, also in cases with a pronounced shoulder in the substhreshold region (fig.5). Without expansive 3D simulations corner devices can be characterised very well. This is important at conditions where neither 2D simulations nor measurements indicate the presence of a corner effect, because no shoulder is observed (e.g. fig.3c). Even at larger drain voltages (V_{dc}=.7V, fig.6) the threshold voltage can be determined.

6. Acknowledgement

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7. Reference

/1/ Technology Modeling Associates, Sunnyvale CA

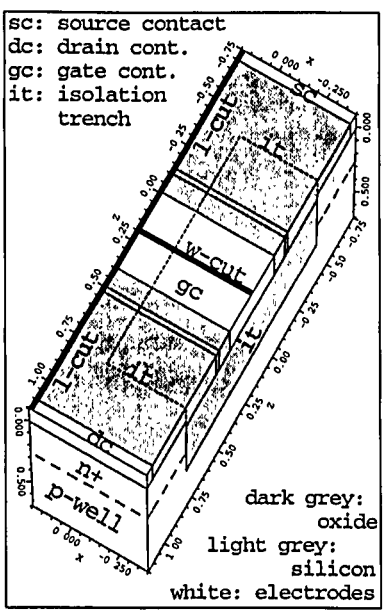

Fig.1: 3D nMOS device, which is symmetric along the plane of the l-cut. Only one half of the device must be simulated. Doping: n^+ source/drain and p-well.

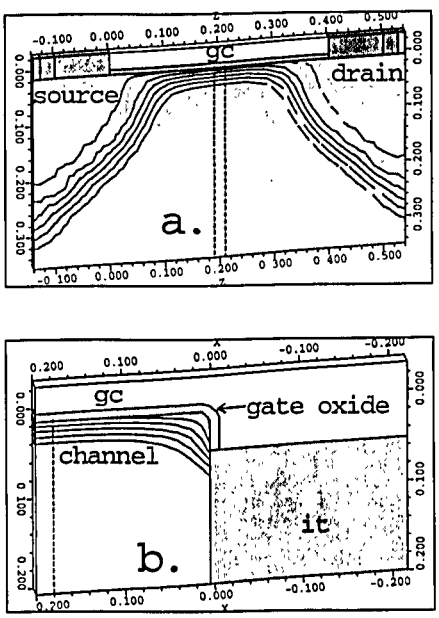

Fig.2a,b: Contourlines of electron density in l-cut (a) and w-cut (b). The positions of both cuts are shown in Fig.1.

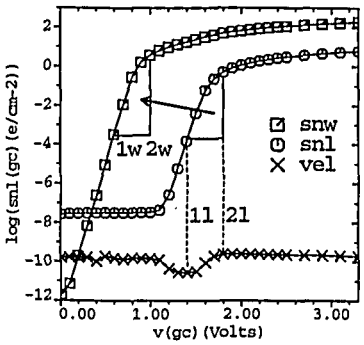

Fig.3a: *snl* according equ.(2), *vel* according equ.(3) and *snw* according equ.(4) in tab.1.

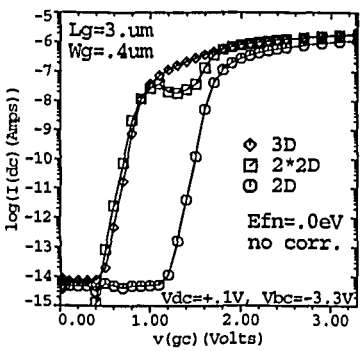

Fig.3b: Drain currents I_{dc} from 2D, 3D and 2*2D simulations (L_g: length and W_g: width of Polygate).

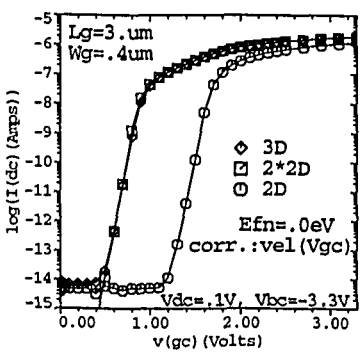

Fig.3c: Currents as in Fig.3b, however $vel(V_{dc})$ was corrected as indicated by the arrow in Fig.3a.

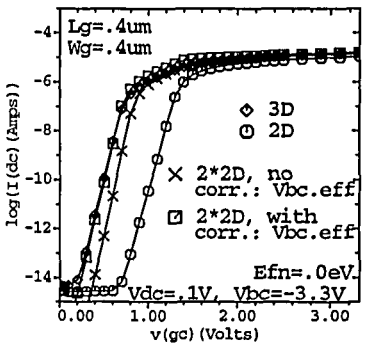

Fig.4: Currents as in Fig.3b. 2*2D results are shown with and without a correction of the bulk voltage V_{bc}.

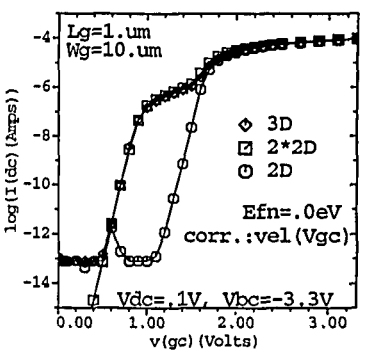

Fig.5: Currents as in Fig.3b, for conditions showing a pronounced shoulder in the subthreshold region.

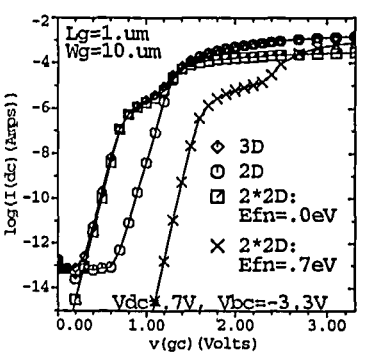

Fig.6: Currents as in Fig.3b for the drain voltage V_{dc}=.7V. 2*2D results are shown for E_{fn}=.0V and E_{fn}=.7V.