On The Modeling Of CV Data For State-Of-The-Art CMOS Technologies: Do We Need To Include Fast Interface States?

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Abstract

In recent publications on MOS devices a fast interface state density has been assumed for standard thermal oxides, which is more than ten times higher than previously expected [2, 7]. In contrast to those results our investigations of standard MOS devices fabricated by three different manufactures do not yield such a high interface state density. Therefore some of the conclusions drawn in [2, 7] appear doubtful. Our results show that fast interface states can still be neglected for modeling state-of-the-art CMOS technologies and previously extracted mobility data are still valid although fast interface states have been ignored.

1. Introduction

CV spectroscopy is widely used for process control and device parameter extraction. Recently the entire 2D doping profile has been determined from extensive CV measurement [1]. A problem of CV spectroscopy is that the interpretation of the CV data is quite complex and can be done in general only by indirect means like inverse modeling. This makes the parameter extraction difficult, sometimes even ambiguous and prone to systematic errors due to inadequate modeling.

In [2] CV spectroscopy is used to determine the number of fast interface states (IS) in MOS devices and it is found that the IS density is much higher than previously thought. The extracted peak IS density is about $5 \cdot 10^{11}/(eVcm^2)$ for standard thermal oxides, which is more than one order of magnitude larger than typically assumed up to now [3]. This implies that the prevailing picture of the Si/SiO_2 interface is wrong and the interface quality is much lower than expected. Moreover, this means that the standard procedure of integrating split-CV data to obtain the mobile channel charge in MOSFETs [4] is flawed, because in weak inversion a large fraction of the channel charge is bound in fast IS and does not contribute to the channel conductivity. Therefore, the mobilities extracted from drain current data under the assumption that all channel charge is mobile are too low. Thus the quality of the de-facto standard mobility-field relation for MOSFETs (see for example [5]), with which nearly all current device simulation models have been calibrated, becomes questionable [2]. In this work an independent evaluation of these effects is attempted.

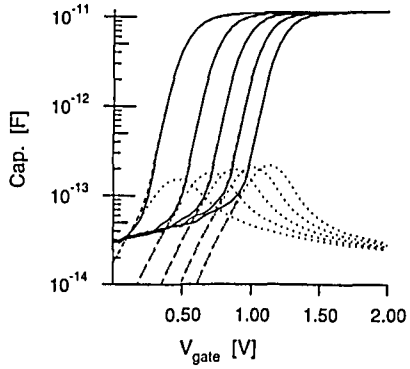

Fig. 1: Measured split-CV data (V_{bulk} = $0V$, $-1V$, $-2V$, $-3V$, $-4V$) (solid lines), simulated results (dashed lines) and partial capacitance due to IS (dotted lines) at room temperature (Siemens).

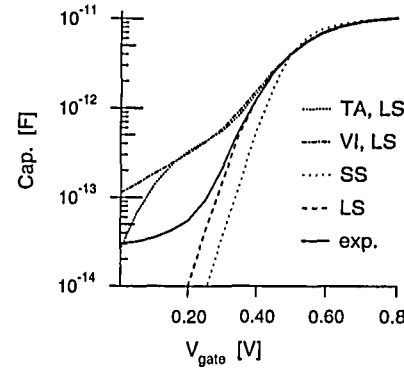

Fig. 2: Measured split-CV data (exp.), simulated without IS using LS analysis (LS), without IS using SS analysis (SS), with IS distribution from [7] (VI) and with IS distribution for [5] from [7] (TA) at room temperature (Siemens).

2. Experiments and Simulation

Standard N^+-poly-gate MOSFETs fabricated at Siemens with an oxide thickness of $6.3nm$ are investigated, which are $50\mu m$ wide and long. All measurements, CV and IV are performed on the *same* transistor for three temperatures (30C, 75C, and 125C). The CV measurements are done with $100mVrms$ small signal voltage at $100kHz$, which is low enough for a quasi-stationary response of fast IS. The IV data are extracted with a drain voltage of $10mV$. In Fig. 1 the measured split-CV data is shown for different back bias voltages (solid lines). The dependency of the split capacitance on back bias confirms that the slowly increasing capacitance in deep sub-threshold is caused by the gate/drain and gate/source overlap. This overlap capacitance is more than one hundred times smaller than the capacitance in strong inversion. This ratio is proportional to the quotient of the channel width and gate area and should be as small as possible to avoid masking of the IS contribution, which is most prominent below threshold voltage. In addition, in Fig. 1 the results of CV simulation are shown (dashed lines). The 1D CV simulations [6] are based on the Schrödinger equation for electrons and holes in the poly-gate and bulk and the Poisson equation including Fermi-Dirac statistics but no incomplete ionization of the dopants in accordance with experiment. Good agreement between simulation and experiment is obtained for all three temperatures (75C and 125C not shown), and the extracted surface doping concentration is $3.7 \cdot 10^{17}/cm^3$. The simulation contains a negligible amount of IS and their corresponding contribution to the split capacitance is also shown in Fig. 1 (dotted lines). Still it is not clear whether this small IS density ($< 5 \cdot 10^{10}/(eVcm^2)$) obtained by inverse modeling is real or not. It could also be an artificial compensation for the neglected overlap capacitance, which can not be included in a 1D simulation. Nevertheless this IS density is much lower than the one found in [2] and it is in accordance with the standard picture.

To further corroborate these findings a more detailed analysis of the split capacitance near the threshold voltage has been performed. In Fig. 2 the experimental capacitance and various simulation results close to the threshold are shown. To achieve a sufficient signal-to-noise ratio a small signal (SS) voltage of $100mVrms$ was used

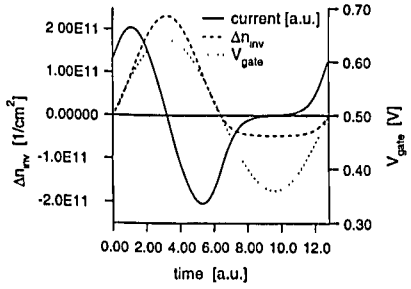

Fig. 3: SS voltage, change in inversion charge and current. ($V_{gate} = 0.5V$, $V_{bulk} = 0V$)

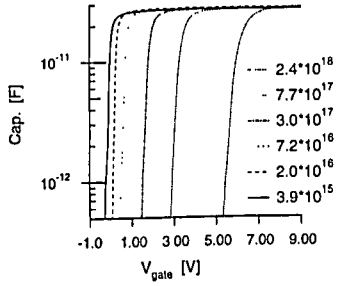

Fig. 4: The original split-CV data of Takagi et al. at room temperature [5] (Toshiba).

in the measurement. But this voltage is too large to apply linear response theory close to or below the threshold. Thus the curve labeled LS in Fig. 2 is calculated using large signal (LS) analysis including all non-linear effects, while the capacitance curve labeled SS is calculated by differentiating the simulated total channel charge with respect to the gate voltage (linear response theory). This is shown in more detail in Fig. 3, where the voltage signal, the inversion charge response and the resulting source/drain current is presented. Obviously the current contains higher order harmonics and the capacitance is calculated by extracting the first harmonic, as it is also done in the measurement process. Please note that the difference between both curves (LS and SS) could easily be mistaken for the impact of IS, which also tend to reduce the second derivative of the CV curve near the threshold. All other results besides the one labeled SS are calculated using LS analysis. To demonstrate the impact of the IS distribution given in [7] in Fig. 2 the corresponding CV curve (VI) is shown. Including this IS distribution the model turns out to be incompatible with our experimental results.

Moreover in [7] the authors propose an IS model for the devices measured in [5] in order to reconcile their results with the ones of [5]. But also this IS density (curve TA in Fig. 2) yields a capacitance which is far too high below threshold. In addition, the characteristic capacitance signature of the IS is not found in the original split-CV data of [5] (Fig. 4), nor does it appear in the split capacitance of devices recently fabricated at Fujitsu (Fig. 5). In Fig. 6 the effective mobility extracted from our measurement under the assumption of a negligible IS density and those of [5] are shown and good agreement is found, while the results of [7] are too low for low effective fields. Due to the unusual high interface state density found in [2, 7] it cannot be expected that the mobility data and the mobility model presented in [7] are generally valid for state-of-the-art CMOS technologies..

3. Conclusion

Our investigation of standard CMOS devices of three different manufactures does not confirm the high number of interface states found in [2, 7] and its impact on effective mobility in heavily-doped MOSFETs. Instead of that the mobilities of [5] are well reproduced without introducing an artificial interface state density as done in [7]. Moreover, we like to emphasize that linear response theory may be invalid for the interpretation of CV data.

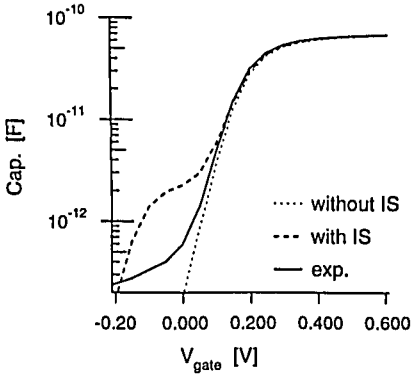

Fig. 5: Split-CV data results for an NMOS device and simulations with and without IS using the model of [7] (Fujitsu).

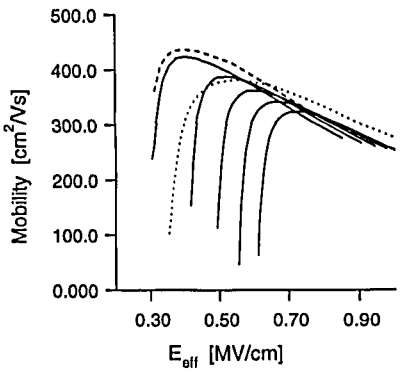

Fig. 6: Effective channel mobility (V_{bulk} = $0V$, $-1V$, $-2V$, $-3V$, $-4V$) (solid lines), the result of Ref. [5] for $3 \cdot 10^{17}/cm^3$ (dashed line) and from [7] for $3.8 \cdot 10^{17}/cm^3$ (dotted line) at $300K$.

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