Modeling Process and Transistor Variation for Circuit Performance Analysis

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Abstract

In this paper, we present a comprehensive TCAD methodology for analyzing the effects of process variation on circuit functionality. We will highlight two essential features of this methodology. First, we will describe the statistical approach we have adopted for worst case file (WCF) analysis in the presence of on-chip variation (OCV). Secondly, we will summarize some key new TCAD statistical modules and analysis tools that support the statistical WCF methodology. The methodology and tools played a critical role in achieving functional first pass silicon, and the desired performance levels for the second generation of DIGITAL's Alpha microprocessors.

1. Introduction

Circuit races and clock skew have become a major design consideration in state-of-the-art digital microprocessors. As such, the ability to accurately assess the impact of process variation on circuit timing has become increasingly critical. In this regard, our experience has shown that OCV is of paramount importance. OCV most directly affects circuit timing because it tends to be systematic (e.g. across field lens aberration, swing curve effects, poly microloading effects during etch). These components of variation directly contribute to the relative path delays of two clock signals into input-output latches and the path of combinational logic between them. Wafer-to-wafer and lot-to-lot process variation, on the other hand, tend to be more random in nature and say little about relative path differences.

Figure 1 illustrates the statistical methodology. In I_{dsat} (saturation current) space, the elliptical and rectangular regions represent expected I_{dsat} performance in the presence of random and systematic (OCV) process variation, respectively. Partitioning variation in this manner is necessary as OCV can affect circuit topology and needs special attention. At each of the 'worst case' corners, device model files for circuit simulation are extracted. However these files do not capture topological effects of process variation on device performance. As a minimum we now provide designers with two model files at each corner (e.g. ss/SS).

Determining how to assign devices different WCF's (ff or FF) in SPICE is often complex. It has forced us to more carefully characterize OCV. Also, our designers and

process development engineers work more closely on agreeing to OCV tolerances. We also had to re-examine the worthiness of using statistical circuit simulation techniques on a select group of critical timing circuits.

Figure 2 shows the circuit delay dependency on OCV parameters for two different circuits: An inverter chain (STD INV), and an N-channel capacitance loaded chain (N-Drain). The N-Drain circuit was designed to highlight the effects of the N-device capacitance including **cgson** the gate overlap capacitance, and **cjswin** the n-device inner sidewall junction capacitance. These linear macromodels illustrate the importance of detailed variational analysis on critical circuits as the behavior of the two circuits are quite different. Depending on the exact magnitude of individual OCV parameters, and their correlations to other parameters, one circuit could meet specifications, while the other would fail.

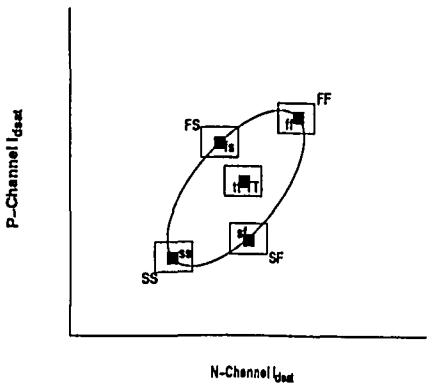

Figure 1: IDSAT Statistical Tolerance Space and WCF Corners with the Corresponding On-Chip Variation Superimposed.

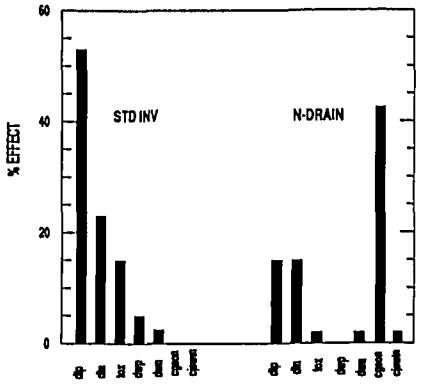

Figure 2: Two SVCC Circuits Risetime Dependency on Basic MOSFET Parameters

2. Statistical Methodology

The foundation of the statistical methodology is accurate characterization and modeling using the limited data typically available at the beginning of a chip design cycle. We use TCAD tools to generate the necessary data for extracting analytical circuit level model parameters at the various WCF corners. The WCF corners are determined by the maximum likelihood probability criteria assuming random variation of the parameters [1].

For OCV modeling, an analytical SPICE model that accurately models physical effects of modern MOSFETs such as quantum mechanical, polydepletion effects, bias dependence of the surface potential, and the overlap capacitance [2] is essential in our approach. The model is predictive within a range of fundamental process parameters and does not require varying non-physical model parameters or determining their ambiguous principal components. The model is thus suitable for statistical design application based on variation in measurable model parameters that provide a

Vector Units	Temperature (^0C)	V_{dd} (V)	Simulated (Nanoseconds)	Measured (Nanoseconds)	Difference (Percent)
Narrow-width inverter	25	2.0	35.7	37.5	5
Standard inverter	25	2.0	40.3	43.4	8
N+ drain	25	2.0	34.6	36.1	5
Gate capacitance	25	2.0	39.6	39.6	0
Interconnect Capacitance	25	2.0	23.0	22.8	-1

Table 1: Comparison of SVCC Measurements to Simulations

direct linkage between circuit and process space. This predictive behavior is used to map OCV parameter variation at each WCF corner as represented by the rectangular region in Figure 1. Within the rectangular regions, device variation is accurately modeled by substituting appropriate values for OCV parameters in the SPICE model file. This parametrized approach facilitates statistical circuit simulation, response surface analysis, and optimization.

3. TCAD Tools

We rely heavily on physically based, properly calibrated TCAD simulation tools for our characterization. In view of the uncertainties associated with two-dimensional process simulation, we resort to inverse modeling techniques [4,6] to extract the 2D doping profile and other geometrical and structural data. With the resultant information, we then use a modified version of the device simulator MINIMOS [3,4] for WCF determination and data generation.

An object-oriented command language based on the Tcl/Tk toolkit [5,6], provides a common interface to all of our TCAD tools. Characterization, modeling and simulation tasks are encapsulated as object methods. This layer of abstraction facilitates the usage of the tools by the novice as well as the expert user. For example, a circuit simulation object is created from its SPICE representation. It is one instance of the more general model object (MO) class that inherits all of its methods. Statistical simulations, analysis of variance, and corner performance analysis can then be performed automatically by invoking the corresponding MO methods.

4. Experimental Circuit Correlation

To further evaluate the overall performance, verify the models, and calibrate our simulation we have found it necessary to develop an extensive set of more than 40 circuits called the SPICE Vector Correlation Circuits (SVCC). These circuits stress different features of the process or design such as capacitance load and different configurations.

First, we note that the effect of OCV variation on experimental correlation can be substantial. We have found that the percent total variation explained by ΔL in models derived from experimental databases is quite lower than what is predicted by simulation based models. We attribute this discrepancy to the uncertainties in ΔL due to the random component of intradie OCV variation. Figure 3 illustrates the results of a simulation experiment that studied the effect of superimposing random Gaussian noise on ΔL values. For zero noise level, the R-square should be unity. As seen, the R-square fit rapidly decreases for a minimal noise magnitude irrespective of the correlation levels.

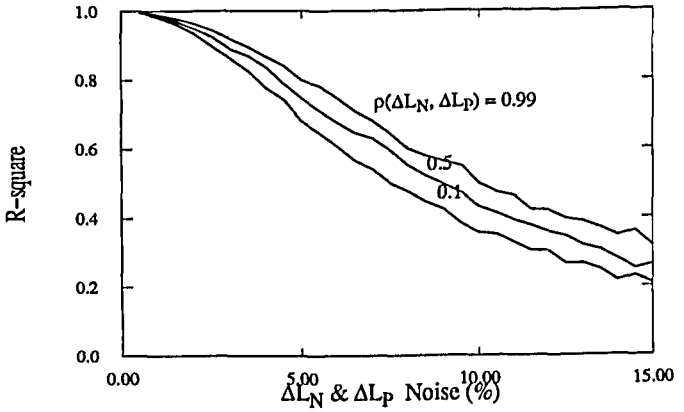

Figure 1: R-Square Regression Model Fit Degradation due to ΔL noise varying the correlation between ΔL_P and ΔL_N.

Careful layout, selection, and processing of the test circuits however, could still result in good correlation between delay measurements on the SVCC circuits and SPICE simulations (See Table 1). These results verify the soundness of the models used. This degree of predictability during early stages of design and process development has proven invaluable.

Acknowledgment

Part of the software development work was done while N. Khalil was pursuing his PhD at the Technical University of Vienna (TUV). The authors would also like to acknowledge the contributions of Professor Siegfried Selberherr at TUV for his continued support and mentoring of TCAD issues at Digital Semiconductor.

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