A Physics Based Resistance Model of the Overlap Regions in LDD-MOSFETs

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Abstract

A new resistance model for lightly doped source/drain regions featuring a non-linear gate voltage dependence has been implemented in the BSIM3 v3 model. This is achieved by separating the LDS(D) resistance into a voltage dependent accumulation and a spreading part.

1. Introduction

In the past much emphasis has been placed on modeling the MOSFET for circuit applications. Contrary to this are the efforts to describe the interconnection resistances of inhomogeniously doped source and drain LDS(D) regions. It has been reported [1] that the source and drain resistances increase with lower gate bias. A method often used to model this effect is to replace the metallurgical channel length by a bias depending effective channel length, or to use a gate bias dependent resistance description.
The aim of this paper is to propose a new resistance model featuring a non-linear gate voltage dependence and using geometric and doping values instead of fitting parameters.

2. Simulation and Discussion

Due to its symmetrical geometry the description of the resistance is focused on the source side of a 0.8 μm MOSFET (fig. 1a). Our simulations show that the resistance from the source contact S to the gate overlap has such a weak bias dependence that an approximation with a voltage independent resistor R_{ext} [2] is sufficient. In the gate overlap region (fig. 1b) the current can be split into two components: **i)** one spreading part which in first order depends on the LDS doping profile and the overlap length l_{ov} only, and one part **ii)** caused by the electron accumulation at the semiconductor-oxide interface induced by the gate bias. In contrary to [3] we propose a parallel resistor network for this region. The total source resistor is therefore

$$R_S = R_{ext} + \left(\frac{1}{R_{acc}} + \frac{1}{R_{spr}} \right)^{-1} + R_{dcpl} \qquad (1)$$

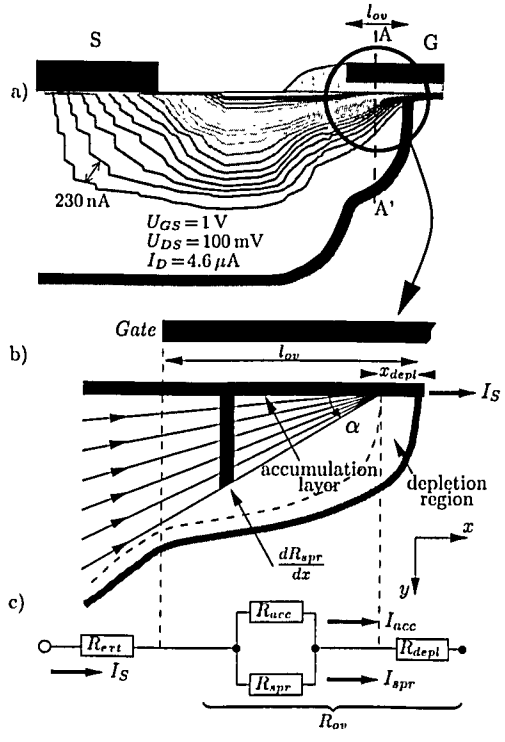

Figure 1: a) Current paths in the source of a MOSFET
b) Model scheme
c) Resistance network of the source region

where R_{depl} represents the resistance of the depletion region at the source side (fig. 1c). Fig. 2 shows the electron distribution for the cross-section A-A' of fig. 1b. Charge density falls sharply within a few nanometers down to doping level concentrations. Therefore it seems appropriate to integrate over the electron distribution and represent the effect as a charge density Q'_{acc} at the SiO_2/Si interface. The charge vanishes at the flat band bias of the overlap region which can be calculated by [1]

$$U_{fb} = \phi_t \ln \frac{N_{Gate}}{N_D} - \frac{Q'_0}{C'_{ox}} \approx 0.15\,V \tag{2}$$

with ϕ_t representing the thermal voltage, N_{Gate} and N_D the gate and LDS doping concentration and Q'_0 the interface states density in the gate oxide with a capacity of C'_{ox}. Various cross-sections in the overlap region yield negligible differences (fig. 3). Therefore the resistance of the accumulation layer can be considered independent of the LDS doping and described by

$$R_{acc}(U_{GS}) = \frac{l_{ov} - x_{depl}}{w \mu_n C'_{ox} (U_{GS} - U_{fb})}. \tag{3}$$

An analogous formula can be found for the resistance of the depletion region:

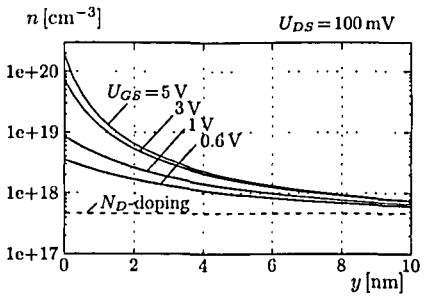

Figure 2: Electron accumulation for a vertical cross-section in the overlap region (neglecting quantum effects)

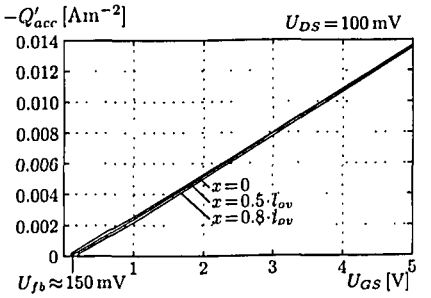

Figure 3: Integrated electron accumulation for various vertical cross-sections in the overlap region

$$R_{depl}(U_{GS}, U_{BS}) = \frac{x_{depl}}{w\mu_n C'_{ox}\,(U_{GS} - U_{fb})} \tag{4}$$

$$\text{with} \quad x_{depl} = \sqrt{\frac{2\,\varepsilon_0 \varepsilon_{si}}{q\bar{N}_D\left(1 + \frac{\bar{N}_D}{N_A}\right)}\left(-U_{BS} + \phi_t \ln\frac{N_A\,\bar{N}_D}{n_i^2}\right)}$$

where $\bar{N}_D$ is the average doping concentration of the LDS region.
The spreading resistance R_{spr} is modeled by considering the geometry of the overlap region (fig. 1b) including a spreading angle α. The result of the parallel connected resistors is:

$$\begin{aligned}
&\left(\frac{1}{R_{acc}(U_{GS})} + \frac{1}{R_{spr}}\right)^{-1} \qquad (5)\\
&= \frac{1}{w\mu_n} \int_{x=0}^{x=l_{ov}-x_{depl}} \frac{1}{C'_{ox}\,(U_{GS} - U_{fb}) + q\bar{N}_D \tan\alpha \cdot x}\, dx\\
&= \frac{1}{w\mu_n q\bar{N}_D \tan\alpha} \ln\left(1 + \frac{q\bar{N}_D \tan\alpha\,(l_{ov} - x_{depl})}{C'_{ox}\,(U_{GS} - U_{fb})}\right)
\end{aligned}$$

Fig. 4 shows the division of the source current I_S into the accumulation and the spreading components according to the above equations.

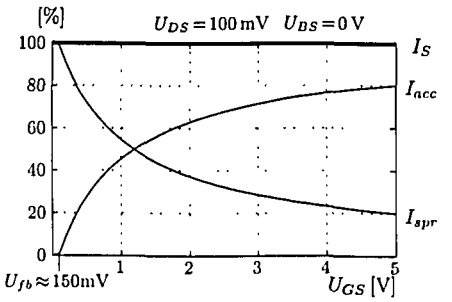

Figure 4: Normalized division of the current into accumulation and spreading components

3. Results

A comparison of the overlap resistance R_{ov} between MEDICI simulation and our proposed model is shown in fig. 5. Moreover, the commonly used description of the popular BSIM3 v3 model [4] is included.
To further verify our model, measurements on a set of 0.8 μm technology MOSFETs have been performed (fig. 6) using the extraction technique described in [5].

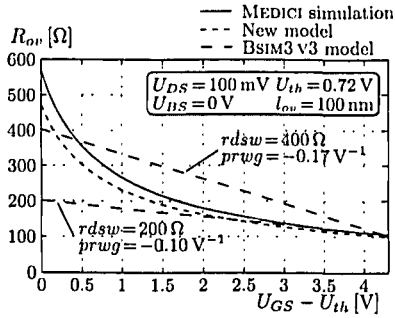

Figure 5: Comparison of the MEDICI simulated overlap resistance with the new model and the BSIM3 v3 model

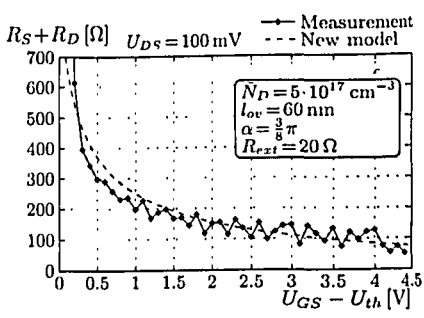

Figure 6: Source and drain resistor measured at MOSFETs with gate lengths between 0.7 and 3 μm and 10 μm gate width [5]

The experiment demonstrates the validity of our proposed model which has been implemented into the BSIM3 v3 model.
SABER-simulations yield differences in the current up to 12% for a 0.25 μm transistor in comparison to the original BSIM3 v3 model. Furthermore, the new model shows a significant improvement in g_m and g_o description which is important for analog simulation.

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References

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