Simulation of Electron Mobility in Ultrathin Fully Depleted Single Gate SOI MOSFETs

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Abstract

Inversion layer mobility in extremely thin SOI MOSFETs with silicon film thickness down to 10 nm has been investigated. The Boltzmann transport equation has been solved by the Monte Carlo method. The mobility decrease appearing in devices with a silicon film thickness below 20nm is satisfactorily explained by the contribution of two scattering mechanisms: i) an increase in phonon scattering as a consequence of the greater confinement of the electrons in the thin silicon film, and ii) the increase in Coulomb scattering due to a greater number of interface traps in the buried $Si\text{-}SiO_2$.

1. Introduction

Electron mobility in SOI MOSFETs with extremely thin silicon films has been experimentally obtained by several authors [1, 2], showing an abrupt mobility decrease in the device if the silicon film thickness is thinner than 20nm. As the explanation of this decrease is still a controversial issue, numerical simulation can provide useful information due to its ability to modify internal variables which are not accessible experimentally.

In the case of silicon films thinner than 20 nm, the thickness of the film is smaller than the width of the inversion charge obtained in thicker films for the same inversion charge concentration. This means that the electron confinement in ultrathin SOI inversion layers is greater than in bulk inversion layers, that is, uncertainty in the location of the electrons in the direction perpendicular to the interface is less in SOI samples than in bulk samples. In accordance with the uncertainty principle, the distribution of the electron's momentum perpendicular to the interface is wider. Taking into account the momentum conservation principle, there are more bulk phonons available which can assist in transitions between electron states, and therefore an increase in the phonon- scattering rate is expected [3, 4]. To prove the above statement, we have calculated the electron mobility in a single-gate SOI MOSFET for different silicon film thickness (T_w). To properly account for electron confinement effects, quantization of electron motion in the thin silicon layer was included in a one-electron Monte Carlo simulator as described in next section. The effects of different scattering mechanisms can be separated and their relative influence on the mobility behavior can be analyzed, which would have been much difficult in experiments.

2. Calculation procedure

Electron quantization in the inversion layer has been properly taken into consideration by self-consistently solving the Poisson and Schroedinger equations. A non-parabolic band model for the silicon has been assumed. Electrons are considered to constitute a two-dimensional gas contained in energy subbands, and transitions between subbands produced by phonon absorption and emission are allowed. Coulomb and surface-roughness scattering processes have also been included. Details of our Monte Carlo procedures can be found in [5]. The structure we have studied consists of an undoped silicon film sandwiched between two oxide layers. The gate oxide thickness was taken as 5nm, while the buried oxide was considered to be 80 nm thick. Under the buried oxide a silicon substrate was assumed. A P^{+}POLY gate was employed. Different thickness values of the silicon film (T_w), ranging from 50 nm to 10 nm, were considered.

3. Results

Mobility has been calculated as a function of the transverse effective field for different silicon film thickness values and for several charged trap concentrations. Fig. 1 shows electron mobility curves calculated at room temperature including phonon, surface-roughness and Coulomb scattering. We have assumed that an interface trap concentration of $N_{it}=5x10^{10}cm^{-2}$ exists in both interfaces. The number in brackets indicates the thickness (in manometers) of the silicon film. As can be observed in this figure, the same mobility behavior as that experimentally observed is obtained, i.e., mobility curves depend slightly on the silicon thickness (T_{wo}) down to 20 NM, while for thinner silicon a stronger dependence is seen. These results have been obtained assuming the same interface charge concentration in both interfaces. Therefore, this means that the greater degradation of the buried interface as responsible for the mobility decrease is not the only effect (nor even the most important) in explaining the behavior experimentally observed. We have also calculated mobility curves but only taken into account phonon and surface-roughness scattering. Fig. 2 shows electron mobility curves for the same samples considered in Fig. 1 but neglecting the effect of Coulomb scattering. As can be seen, the narrower the Is film, the lower the electron mobility at low inversion electron concentrations, where phonon scattering is the main scattering mechanism (if Coulomb scattering is not present). Therefore, these results corroborate the contribution of phonon scattering to the mobility degradation as T_{wo} decreases.

To test the explanation suggested by Torii et al [2], we have also studied the role played by the high concentration of interface trap density, N_{it}, in the back interface (buried oxide) in the degradation of the electron mobility as the silicon layer thickness decreases. To do so, we have assumed that the interface trap concentration in the buried interface is $N_{it}=5x10^{11}cm^{-2}$, while the interface trap concentration in the gate interface has been assumed to be the same as before. Fig. 3 shows the mobility curves in this case. As was expected, a greater separation between mobility curves at low transverse electric fields is observed. This fact indicates that the greater degradation of the buried interface also contributes to explaining the mobility decrease observed experimentally.

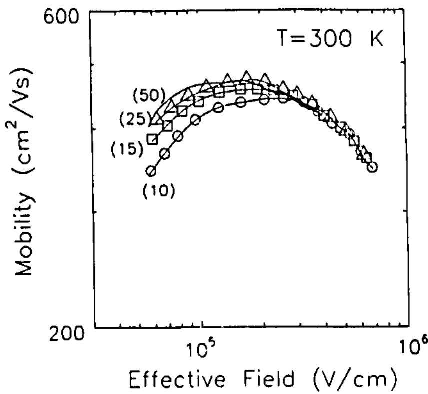

Fig.1.- Electron mobility curves for different Si film thickness values (labels in nm). An interface trap concentration of 5×10^{10} cm^{-2} is assumed at both interfaces.

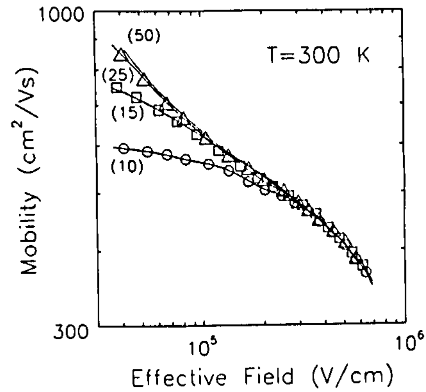

Fig2.- Electron mobility curves neglecting the effect of coulomb scattering. Both phonon and surface-roughness scattering are considered.

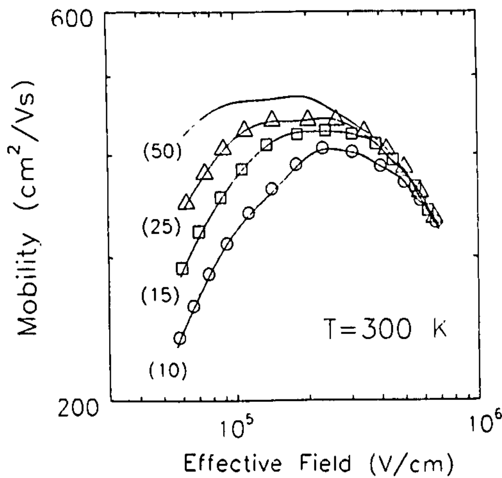

Fig. 3.- Mobility curves for various Si film thickness values, with different interface-trap concentrations in the two interfaces ($N_{it}=5 \times 10^{10}$ cm^{-2} in the top interface, and $N_{it}=5 \times 10^{11}$ cm^{-2} in the back interface)

4. Conclusions

To sum up, we have shown that both phonon scattering and the greater interface trap concentration in the buried oxide contribute to the mobility degradation as the silicon film thickness is reduced, and these explanations are therefore complementary in this sense. Nevertheless, note that while the Coulomb limitation is a consequence of technological problems (and therefore, expected to be overcome in the near future), the other reason (phonon limitation) is intrinsically linked to the very thin SOI devices, and is therefore only avoidable at very low temperatures (4.2 K).

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