Simulation based development of EEPROM devices within a 0.35μm process

R. Duffy[a], A. Concannon[a], A. Mathewson[a], C. de Graaf[b], M. Slotboom[b], R. Verhaar[b]

[a]National Microelectronics Research Centre,
Lee Maltings, Prospect Row, Cork, Ireland.
[b]Philips Research Laboratories,
Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands.

Abstract

This paper outlines the capabilities of 2D process and device simulation in the development of byte-erasable EEPROMs within a 0.35μm CMOS process. Evaluation of different cell options, investigation of critical design rules and process development have been successfully undertaken. Simulation has been shown to provide useful insight and understanding that cannot be obtained from measurements alone and can increase the speed of the design cycle.

1. Introduction

The overall aim of this work was to undertake the simulation of EEPROM structures within a 0.35μm CMOS process. The TMA simulation software was used, which included the 1D and 2D process simulators SUPREM3 and TSUPREM4, while the 2D device simulator was MEDICI. A review of several methodologies for the use of numerical simulation in NVM development has been performed [1]. The most appropriate approach was used to evaluate the embedded byte-erasable EEPROM which relies on Fowler-Nordheim tunnelling for both programming and erasing. Calibration of the simulators is very important and once achieved, investigative simulations can be successfully carried out. Different cell options can be examined and comparisons made between alternative cell designs. Furthermore a calibrated simulator can enable process variations to be investigated and process splits simulated.

2. Simulation Methodology and Issues

Prior to EEPROM investigation, the simulation methodology required calibration of the baseline CMOS process. Low and high voltage MOS transistor electrical characteristics were extensively modelled and calibrated. Fowler-Nordheim and band to band tunnelling parameter extractions were performed using tunnel capacitor measurements and simulations. Fig.3 shows an example of the results generated after the Fowler-Nordheim parameter extraction phase.

Considerable effort was made solving problems and debugging simulations during the modelling of the EEPROM structures, to obtain reliable and trustworthy simulation results. Mesh regrids on important physical quantities such as doping and band to band tunnelling generation were found to be essential. It was also discovered that default mesh generation techniques produced insufficent mesh in the oxide regions of the simulated EEPROMs. While DC characteristics remained accurate, transient characteristics were significantly affected. Careful definition of mesh in these regions significantly reduced inaccuracies in simulated transient results.

3. EEPROM Simulations

After the calibration and parameter extraction procedures had been completed, attention was turned to investigative simulations. A comparison was made between two alternative EEPROM cell designs. The schematic cross sections and layouts, which represent the memory part of the cells, are shown in Fig.1 and Fig.2. The control gate, floating gate, injector implant, tunnel oxide and active area masks are clearly labelled. Comparing the two layouts it should be noted that Cell B has an irregularly shaped floating gate and that the injector implant mask edge corresponds to the tunnel oxide mask edge. During processing it was seen that due to misalignment errors, the overlap of the injector implant mask with the tunnel oxide mask could vary significantly. This overlap is a critical dimension in these EEPROM cells, and is labelled in Fig.1. Measurements showed that cells on adjacent word lines had quite different programming speeds, with Cell A being more affected than Cell B. Simulation experiments were thus undertaken to investigate the causes and the extent of these problems.

Fig.4 shows Cell A programming simulations for mask overlap values of 0.2μm and 0.0μm. It was seen that a smaller overlap resulted in slower programming, since the tunnel current is lower. Further investigation indicated greater power consumption for the 0.0μm case, as the substrate current is approximately three orders of magnitude higher. These results are explained with the aid of the plots in Fig.5 and Fig.6. Comparing the Cell A case with the Cell B case it can be seen that a significantly larger depletion region forms under the tunnel oxide region of Cell A during programming. For smaller Cell A mask overlaps, a thicker depletion region was observed. The resulting potential drop associated with this depletion region, produced a greater drain decoupling from the floating gate. This was observed to produce a slower programming characteristic [2]. Cell B was then simulated, but as expected it was seen that there was no significant change in the depletion regions or in the decoupling of the drain from the floating gate due to this misalignment effect. The presence of an LDD implant self aligned to the floating gate and the increased distance between the tunnelling region and the drain junction in the Cell B design accounted for this more desirable characteristic.

Measurements indicated that for both Cell A and Cell B a higher injector implant dose provided faster programming and erasing characteristics. Fig.7 and Fig.8 show simulated and measured results for injector implant splits. The default implant was Phosphorus of dose $5e13cm^{-2}$ at 40keV. The output characteristic of interest was the V_t window (ΔV_t), which is the difference between programmed V_t and erased V_t. In the cases displayed in the figures a default overlap of 0.1μm was simulated. With respect to Cell A in Fig.7 there is a large distribution in the measured ΔV_t, due to the previously mentioned processing issue involving the mask overlap misalignment. From simulations similar to those in Fig.4 it was determined that the 0.1μm overlap case for Cell A had a relatively fast programming characteristic, thus the simulated

ΔV_t here should correspond to the top of the measured ΔV_t range. The simulated values of ΔV_t follow the top of the measured range quite well. The results for Cell B are shown in Fig.8. Cell B does not suffer from the overlap misalignment processing issue, as reflected by the smaller measured ΔV_t range. In this case the simulated Cell B characteristics should simply be within the measured range. Again it can be seen that these results follow the measurements quite well. Overall good agreement with measurements was achieved for these simulated process splits and as a result it was concluded that the simulators could be used to predict the effect of process options on the cell characteristics.

4. Summary

The role of simulation in the devlopment of EEPROMs within a 0.35μm CMOS process has been presented. A comparison between different cell types has been made, evaluation of critical dimensions has been achieved, and simulated process splits have been validated by good agreement with measurements. This provides confidence in simulation driven investigation into process options and possible optimisation of device design.

References

[1] R. Duffy, "Numerical Simulation of Non-Volatile Memory Technology," *M.Eng.Sc. thesis*, National University of Ireland, 1996.

[2] A. Kolodny et al, "Analysis and Modeling of Floating-Gate EEPROM Cells," *IEEE Trans. El. Dev.*, vol. ED-33, pp. 835-844, 1986.

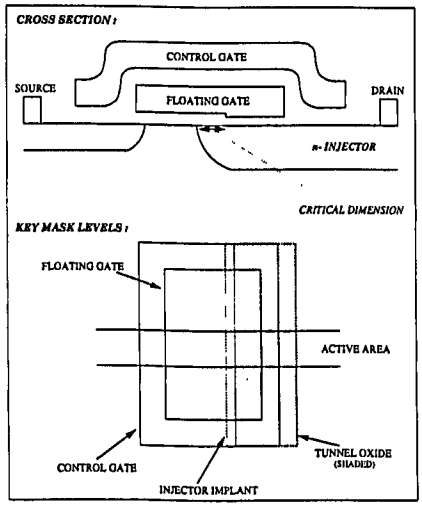

Figure 1: Schematic diagrams representing the EEPROM Cell A cross section and layout. The select transistor is not shown.

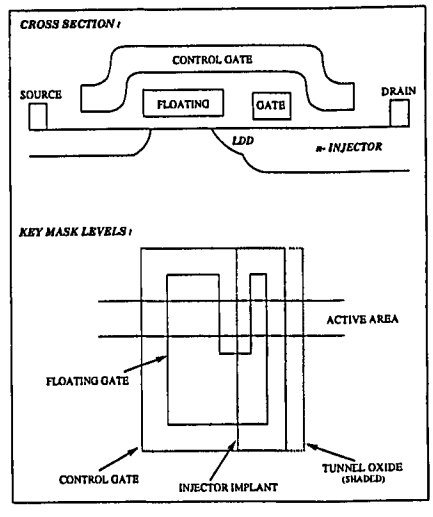

Figure 2: Schematic diagram representing the EEPROM Cell B cross section and layout. The select transistor is not shown.

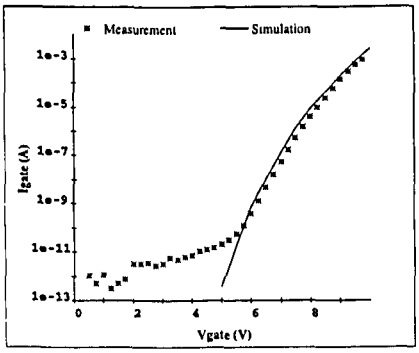

Figure 3: Measured and simulated tunnel current for a tunnel capacitor after the extraction of the silicon to poly Fowler-Nordheim tunnelling coefficients.

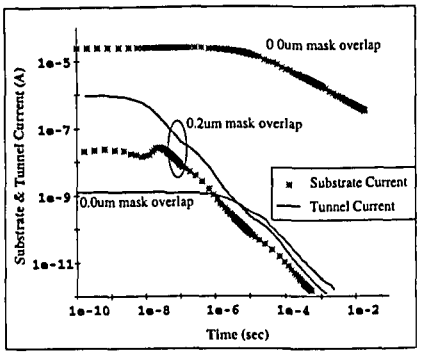

Figure 4: Simulated programming of EEPROM Cell A for different tunnel oxide mask-injector implant mask overlaps, substrate and tunnel current vs time, Vd=13V.

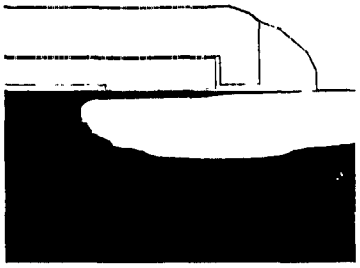

Figure 5: Plot of simulated depletion region (grey area) for Cell A during programming at t=1ms.

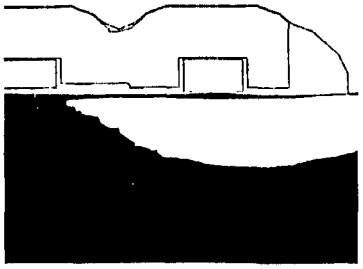

Figure 6: Plot of simulated depletion region (grey area) for Cell B during programming at t=1ms.

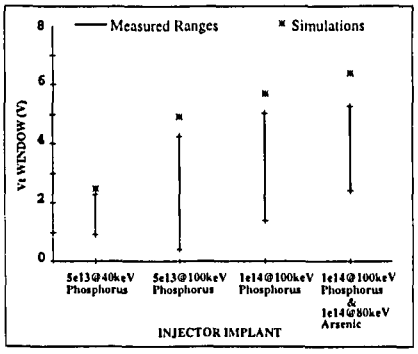

Figure 7: Cell A simulations and measurements for injector variation. V_t window vs injector implant, Vpp=12V, tp=1ms.

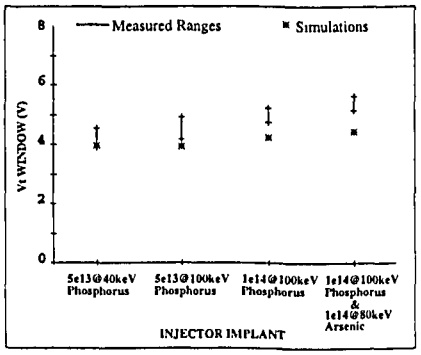

Figure 8: Cell B simulations and measurements for injector variation. V_t window vs injector implant, Vpp=12V, tp=1ms.