Influence of the Ge concentration on the threshold voltage and subthreshold slope of nanoscale vertical Si/SiGe pMOSFETs

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Abstract

An analytical model has been set up to investigate the influence of SiGe in the source on the threshold voltage and subthreshold behaviour of heterojunction pMOSFETs. The use of SiGe in the source region of the pMOSFET introduces an extra degree of freedom for fine-tuning of the subthreshold and on-state behaviour of the devices. It will be shown that the short channel behaviour of these devices is greatly improved in comparison with vertical homojunction Si structures. Careful design and optimisation of these devices show that the use of Ge is only advantageous for sub 0.1 μm devices. Structures with channel lengths down to 30 nm exhibit promising characteristics.

1. Introduction

The use of strained SiGe layers in the design of MOSFET structures gives the opportunity to vary the bandgap by varying the concentration of germanium. Bandgap engineering is an important tool to optimise transistor characteristics [1][2] especially when channel lengths reach the sub 0.1 μm regime. One of the most important short channel effects (SCE) in short channel devices is the threshold voltage roll-off and the subthreshold slope roll-up. In the p-channel device, presented in this paper [3], a material dependent barrier between source and channel is inserted to lower the SCE. The gate action on a lowly doped SiGe region of the source, near the channel, is used to lower the effective barrier for the carriers and to cause a large current to flow in the on-state of the MOSFET. Figure 1 gives a schematic view of the vertical heterojunction pMOSFET. Rather then using channel engineering to optimize the transistor characteristics we use source engineering. The threshold voltage, subthreshold slope, off-state current and on-state current largely depend on the molefraction of the SiGe layer. The calculation of potential and current has been discussed extensively in [4].

This study already showed the promising characteristics of the device. In this paper the emphasis lies on the influence of the SiGe source layer on the threshold voltage and the subthreshold behaviour. It will be shown that the V_T roll-off can be substantially decreased by using Ge in the source, even for extremely small devices down to 30 nm. The subthreshold slope is improved in comparison with homojunction pMOSFETs, but only for sub 0.1 μm devices.

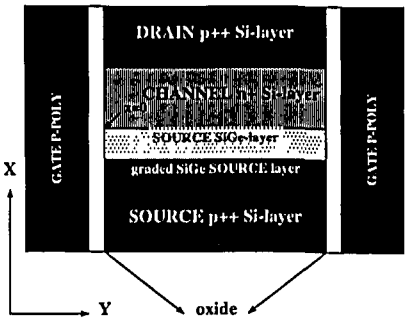

Figure 1: Schematic view of the Si/SiGe vertical pMOSFET

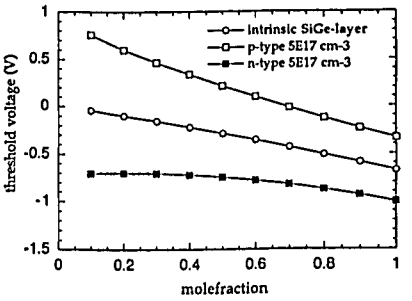

Figure 2: V_T as a function of the molefraction for different doping concentrations of the SiGe-layer

2. Modeling

2.1. Long channel theory

For long channel heterojunction pMOSFETs the assumption $L_{sige} << L_{si}$ is made. The channel potential is independent of x and the threshold voltage is defined as the gate voltage at which the hole concentration in the channel has become equal to the n-type doping concentration. This definition leads to the following expression for V_T:

$$V_T = V_{FB} - \xi - \gamma\sqrt{\xi} \tag{1}$$

$$\xi = V_{bi1} + \chi_{si} - \chi_{sige} + \frac{E_{gsi}}{2q} - \frac{E_{gsige}}{q} + \frac{kT}{q} ln(\frac{N_{si}}{n_{isi}} \frac{N_{vsige}}{N_{SD}} \sqrt{\frac{N_{csi}}{N_{vsi}}}) \tag{2}$$

$$V_{FB} = \frac{-E_{gpoly}}{q} - \frac{kT}{q} ln(\frac{N_{si}}{N_{csi}}) \tag{3}$$

where χ=electron affinity, γ=body factor of the Si channel and V_{bi1}=built-in potential between the highly doped source region and the lowly doped region. Term ξ can be written as $2\phi_F$ in case of a Si-only transistor.

The subthreshold slope is calculated using the current expression in [4]:

$$I_p = q\mu_{psi} V_{th} \frac{W}{L} \frac{N_{vsi} N_{SD}}{N_{vsige}} exp(\frac{-V_{bi1}}{V_{th}}) exp(\frac{-E_B}{kT}) (exp(\frac{V_{DS}}{V_{th}}) - 1) \int_0^\infty exp(\frac{-\psi_{si}(y)}{V_{th}}) dy \tag{4}$$

$$S = V_{th} ln(10)(1 + \frac{C_{si}}{C_{sige}})(\frac{1}{\frac{V_{th}}{2\psi_{si}^o} - 1}) \tag{5}$$

2.2. Short channel theory

In case of short channel devices, the channel potential expression contains a combination of two natural lengths λ_1 and λ_2, where the former is related to the SiGe

source layer and the latter to the Si channel. For calculation of the short channel subthreshold slope the current expression derived in [4] was used. The threshold voltage is defined as the gate voltage at which inversion is reached at x=0, the place in the channel closest to the source, reaches inversion. The equations for subthreshold slope and threshold voltage derived in this way are quite complex and were evaluated with Mathematica.

3. Discussion

Eq. 1 is strongly dependent on the molefraction of the SiGe-layer, doping concentration of the Si channel and doping concentration of the SiGe source layer. Figure 2 shows the dependence of the threshold voltage on the molefraction for different doping concentrations of the SiGe source layer. Figure 3 shows the dependence on channel doping for both Si-only devices and Si/SiGe devices. The Ge-concentration makes V_T more negative but less sensitive towards drain bias and channel length, which can be seen from figure 4. The threshold voltage dependence on L is substantially reduced by the use of the SiGe source layer. The same conclusion can be made for the subthreshold slope. The subthreshold slope roll-up is reduced by the SiGe. However, this is only true for the short channel devices. Eq. 5 is almost independent of the Ge molefraction. This can also be seen in figure 5. As can be seen from figure 6 very high Ge-concentrations will degrade the subthreshold slope.

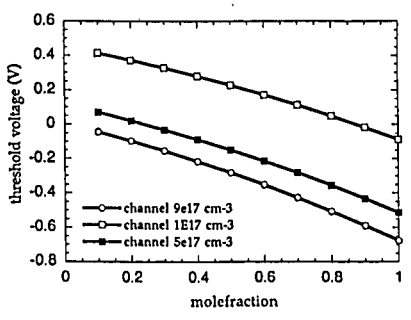

Figure 3: V_T as a function of the channel doping

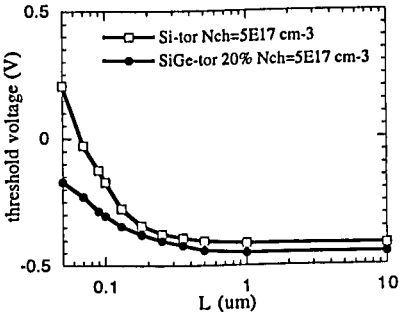

Figure 4: V_T as a function of the channel length

The derived equations are important first order tools in the design and optimisation of the vertical heterojunction pMOSFETs. 2D numerical simulators were used to investigate the behaviour of the sub 100 nm devices. The results show that the use of a moderate Ge-concentration in the source region of the pMOSFET reduces the amount of channel doping needed to meet the specifications taken from [5]. Lower off-state currents can be achieved with higher Ge-concentrations. However, this leads to a degradation of the subthreshold slope and a threshold voltage which is too low. Significant improvement in device characteristics can be seen for the shortest channels. This improvement becomes smaller for the long channel devices. For channel lengths down to 30 nm off-state currents around 1nA/μm are achieved while the Si-only transistor shows complete punchthrough.

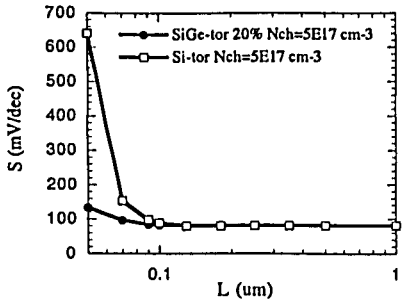

Figure 5: S as a function of the channel length

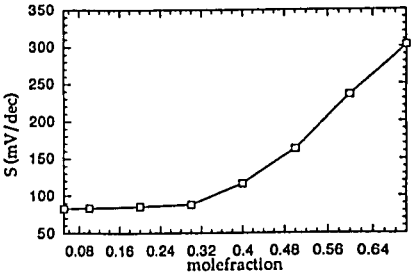

Figure 6: S as function of the Ge molefraction

4. Conclusion

We have investigated the device behaviour of Si/SiGe pMOSFETs. Analytical models for threshold voltage and subthreshold slope have been set up and it was shown that the use of SiGe in the source region of these devices suppresses the V_T roll-off and the roll-up of the subthreshold slope substantially. This effect is more pronounced for short channel devices. Optimally designed pMOSFETs show that the use of moderate Ge-concentrations is the best trade-off. These Si/SiGe devices exhibit improved device characteristics towards the homojunction Si devices, even for channel lengths down to 30 nm.

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References

[1] M. Yoshimi, M. Terauchi, A. Murakoshi, M. Takahashi, K. Matsuzawa, N. Shigyo and Y. Ushiku, "Technology Trends of Silicon-On-Insulator - Its Advantages and Problems to be Solved," *IEDM*, pp. 429-432, 1994.

[2] S.A. Hareland, A.F. Tash and C.M. Maziar, "New structural approach for reducing punchthrough current in deep submicrometre MOSFETs and extending MOSFET scaling," *Electronics Letters*, vol. 29, no. 21, pp. 1894-1895, 1993.

[3] U.S. Provisional Patent Application Number: 60/001,022; July 7th, 1995, C.J.R.P. Augusto, IMEC.

[4] N. Collaert and K. De Meyer, "Current calculation of a submicron Si/SiGe heterojunction MOSFET," *Proceedings of the International Semiconductor Device Research Symposium*, pp. 517-520, 1997.

[5] SIA roadmap, Semiconductor Industry Association, 1997.