Minimizing Bitline Coupling Noise in DRAM with Capacitor-Equiplanar-to-Bitline (CEB) Cell Structure

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Abstract

A new scheme of stack DRAM referred to as Capacitor-Equiplanar-to-Bitline (CEB) is proposed for minimizing bit-line coupling noises. The cell capacitors are fabricated in between bit-lines, so that the bit-line coupling is blocked by the node capacitor and shielded by the plate. 3D simulation shows that the bit-line coupling noise is almost eliminated (<1% of total bit-line capacitance) in CEB scheme. The SPICE simulation shows ~3ns faster bit-line signal sensing in 0.25μm 64Mb CMOS DRAM. The CEB scheme also leads to smaller topology and simpler fabrication process.

Introduction

A typical stack DRAM cell [1] is composed of one n-MOS pass transistor and one stack capacitor for storing charges. In order to maintain large enough signal-to-noise (S/N) ratio, the cell capacitance needs to be ~30fF. The stack capacitor is typically fabricated before bit-line formation in 4Mb DRAM or earlier and is known as Capacitor-Under-Bitline (CUB) scheme. As DRAM scaling continues, the CUB scheme becomes increasingly difficult for maintaining large enough capacitance. In 16Mb DRAM or newer generations [2], the capacitor is commonly fabricated after the formation of bit-line, as known as Capacitor-Over-Bitline (COB) scheme. In COB scheme, the

node capacitor can be high and can utilize the space above bit-line for larger capacitance. Both CUB and COB schemes result in large capacitor topology, which causes process difficulties (e.g. high aspec ratio contacts, planarization, ...etc.). Furthermore, both CUB and COB schemes suffer bit-line coupling noise, which is one of the most serious problems for future DRAMs [3-6].

3D Structure of $8F^2$ Cell

The $8F^2$ cell [7] with either COB or CUB scheme can not enlarge the capacitor footprint by taking advantage of the space over or under bit-lines as limited by the lithography resolution (i.e. F). A 3D structure of $8F^2$ DRAM cell with crown-like capacitor has been developed for simulation. The cross-section of the cell structure with COB, CEB, and CUB is sketched in Fig.1. The bit-line and crown capacitor are connected through poly plugs with height of C_{1h} and C_{2h} respectively. By varying C_{1h} (or the bitline-to-plate distance d in Fig.1), the bit-line coupling capacitance of various schemes can be simulated [9] using reflective boundary conditions on the 3D capacitance solver Raphael RC3 (Version 4.0). The cell size is $4F \times 2F$ ($=8F^2$) with a crown-like capacitor of ~30fF. The bit-line junction capacitance is not included in this simulation.

Bit-line Coupling Capacitance Simulation

The 3D simulated bitline-to-bitline coupling capacitance C_{blbl} of COB, CEB, and CUB schemes is shown in Fig.2a. Clearly, the CEB scheme results in minimal C_{blbl}, a result from the blocking of electric field lines by the node capacitor and the shielding by the plate. This would minimize bit-line coupling capacitance to a negligible level, although the bit-line to plate capacitance increases. There is no capacitor blocking in COB or CUB schemes, therefore, the bit-line coupling capacitance is larger as shown in Fig.2a. The total bit-line capacitance (not including junction capacitance) as well as various capacitance components are shown in Fig.2b, where the CEB scheme results in the lowest coupling but higher total bit-line capacitance. When the bit-line is closer to the metal layer in CUB scheme, the total bit-line capacitance increases due to metal shielding effect (i.e. termination of field lines from bit-line to metal).

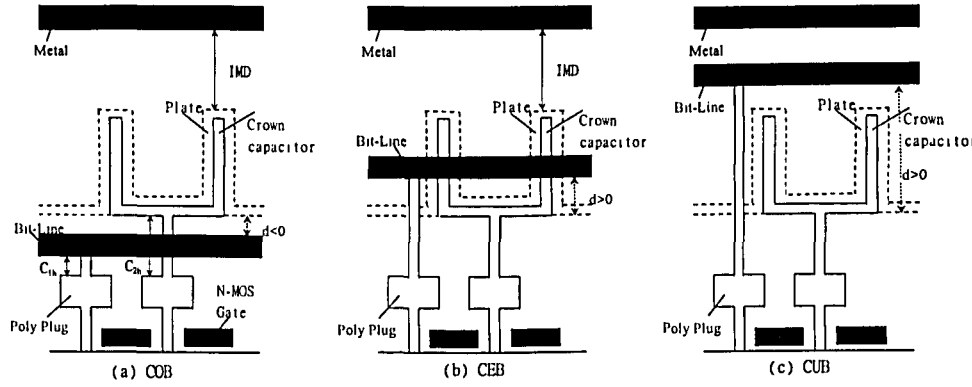

Fig1: Cross-section of 3D structure of $8F^2$ DRAM cell with crown-like capacitor in COB (a), CEB (b), and CUB (c) schemes.

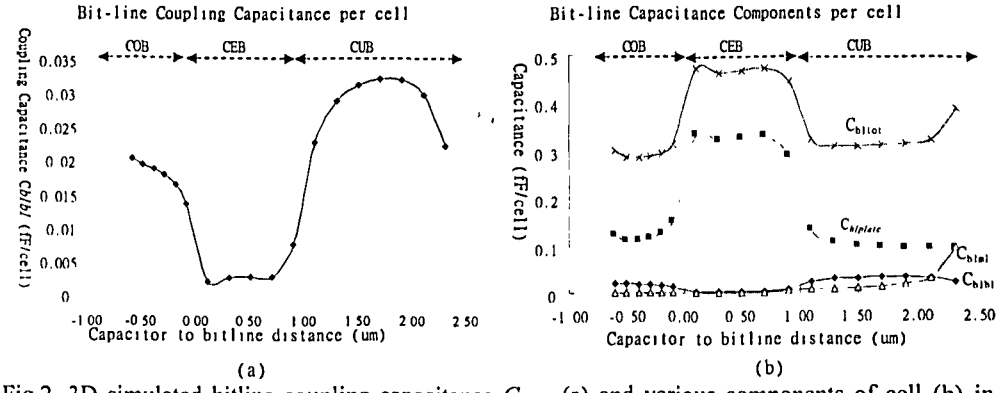

Fig.2. 3D simulated bitline coupling capacitance C_{blbl} (a) and various components of cell (b) in COB, CEB, and CUB schemes. The total bit-line capacitance does not include junction capacitance.

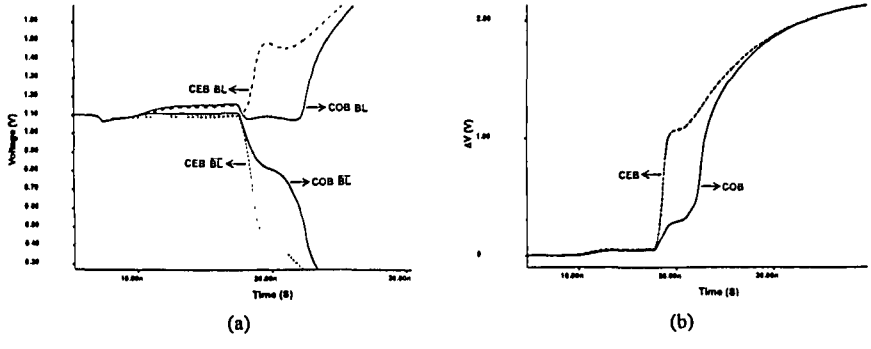

Fig.3: The bit-line pair potentials (a) after sense amplifier activation and differential bit-line signal (b) in CEB and COB schemes for comparison.

Bit-line Signal Simulation

A SPICE simulation of array with COB and CEB schemes is shown in Fig.3 with 256 cells in a bit-line and including both inter- and intra-bitline couplings. Cell and transistor models are calibrated on a stacked 0.25μm CMOS DRAM technology. Fig.3a shows the bit-line pair potentials after activating sense amplifier are separated faster by ~3ns with the new CEB scheme than COB scheme. Fig.3b shows the differential bit-line signal in CEB and COB scheme for comparison.

Conclusions

In this paper we propose a new CEB scheme for minimizing bitline coupling noises. 3D simulation shows that the bit-line coupling capacitance in CEB is almost eliminated by capacitor blocking and plate shielding. The SPICE simulation shows that CEB results in >3ns faster bit-line signal sensing than other schemes. The CEB scheme leads to smaller capacitor topology and simpler fabrication process significantly.

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