Influence of the S/D architecture on the V_T of deep submicron MOSFETs

Serge Biesemans[a] and Kristin De Meyer[a,b]

[a] ASP-division, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
[b] ESAT, KULeuven, Kardinaal Mercierlaan 94, B-3001 Leuven, Belgium

Abstract

In this paper, the influence of the source/drain (S/D) architecture on the short channel effect (SCE) and the device performance (through R_S) is investigated using both experimental and simulation results. While most existing models relate the SCE and performance only to the oxide thickness (T_{OX}) and substrate doping (N_{sub}), we show that there exists a universal curve for the threshold voltage roll-off (ΔV_T) for various different S/D profiles. The question of which 'L' should be taken in SCE models is addressed.

Introduction

As MOSFET devices continue to shrink, the ability to simulate correctly the device characteristics becomes more difficult. Especially for devices with channel lengths around 100 nm, the accuracy with which the material thickness and the doping profiles have to be known, is very high. The SIMS technique can provide vertical doping profiles with an accuracy as good as 5%. However, no direct information is available by using a physical characterization technique to gain information of the exact 2D profile of the S/D structure, although some effort is undertaken. Furthermore, the dependence of the lateral S/D profile on the SCE has not been investigated at all. While most SCE models for the V_T include correctly T_{ox} and N_{sub}, no information regarding the lateral S/D junction profile is included.
Here, we use the results of the work of [1] where a calibration of the device simulator MEDICI was undertaken. A good quantitative agreement with experiment for a complete L-array, for poly gate lengths ranging from 10 μm down to 0.08 μm, has been achieved. The simulations performed are done for nMOSFETs with 5 nm gate oxide. The main parameter for bookkeeping is the metallurgical channel length L_{met}. The same vertical As extension profile has been used but with different values for the ratio R, shown in Fig.1. Although this procedure of creating a 2D n+ profile out of a 1D SIMS profile is somewhat arbitrary, it is ideal for studying its result on the device characteristics. It can answer the questions like 'what happens if I make my profile steeper ?", or "what is an optimum S/D profile ?"

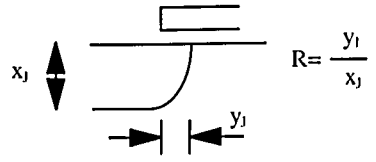

Fig.1 The ratio R quantifies how far a certain vertical doping profile extends laterally

This investigation can then be followed by a study using a process simulator in order to find the process conditions to be able to actually fabricate the optimum S/D profile.

The physical gate length L_g has been adapted so to end up with the same L_{met}. The lateral doping profiles for 4 ratios (R=0.1/0.3/0.5/1.0) are shown in Fig.2 for a device of L_{met}=120 nm. The influence of the steepness of the lateral doping profile on the SCE and the parasitic S/D resistance (R_S) will be investigated next.

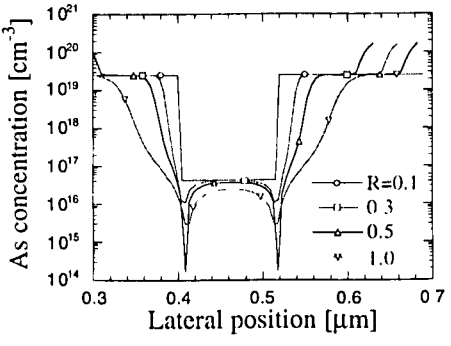

Fig.2 Four different lateral doping profiles used to study the influence of the steepness of the profile

Results and discussion

We use a modified Shift&Ratio algorithm [2], [3] to extract the V_T, the effective channel length L_{eff} and the R_S from the I_{ds}-V_{gs} characteristics in the linear regime (V_{ds}=20 mV). We start by reporting the results for experimentally made nMOSFET [4]. Two devices are taken who are identical except in the As extension dose. Device 'A has a dose of 1E14 cm^{-2} while device 'B' has a dose of 9E14 cm^{-2}. Fig.3 (left) shows the extracted V_T as a function of the physical poly Si gate length L_g while Fig.3 (right) plots the same data but as a function of the electrical channel length L_{eff}. It can be seen that, although the difference in dose is nearly one order of magnitude, the data follow essentially one and the same curve. The authors do not know of any model analytical model which can distinguish between the two cases of Fig.3. As a result, this phenomenon is not entirely understood. It is clear that L_{eff} is the important parameter which serves the same importance as E_{eff} for the universal mobility curve. The L_{eff} parameters

contains the information of the lateral S/D profile and can be determined through I_{ds}-V_{gs} measurements.

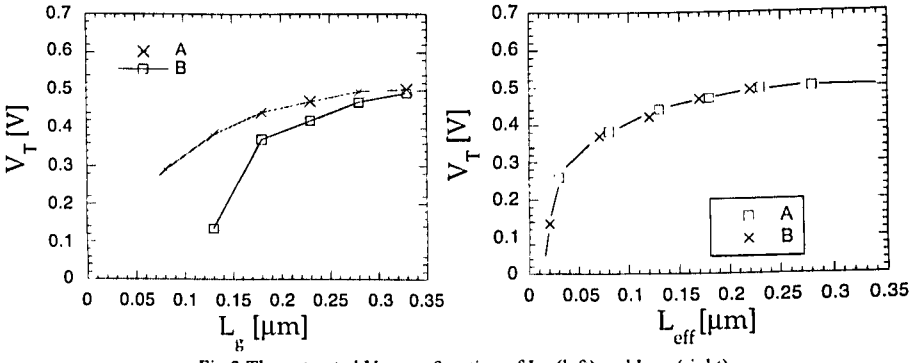

Fig.3 The extracted V_T as a function of L_g (left) and L_{eff} (right)

Next, we will try to reproduce this result using simulation data with the profiles of Fig.2. The results of the V_T extraction in the linear regime are shown in Fig.4 as a function of L_g, L_{eff} and L_{met}. Only as a function of L_{eff}, we obtain a universal V_T-L_{eff} curve. This indicates that in the SCE models, it is the L_{eff} which has to be used and not L_g or L_{met}. Under normal circumstances, $L_{met}<L_{eff}<L_g$.

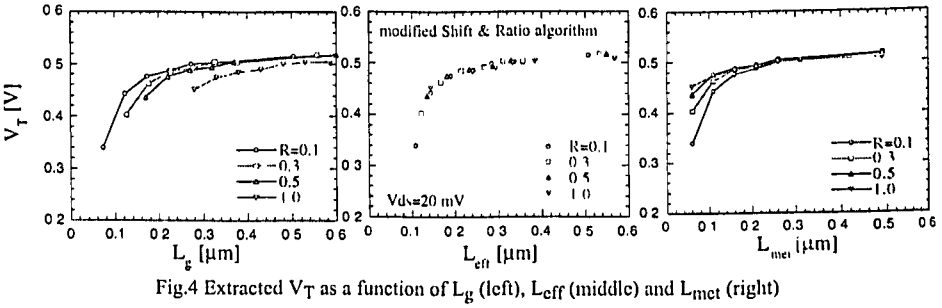

Fig.4 Extracted V_T as a function of L_g (left), L_{eff} (middle) and L_{met} (right)

It is interesting to note that for a fixed L_{met}, it is preferable to have less steep profiles. In this way, the depletion layer depth created by the S/D spans mainly the S/D area itself and penetrates less the electrical channel.

To investigate the influence of the lateral S/D profile on the device performance, we have plotted the I_{ds} and the extracted R_s in Fig. 5 for L_{met}=0.12 μm and V_{ds}=20 mV.
The R_s has different contributions like contact, diffusion, spreading and accumulation resistance [5]. The difference between the various profiles can be fully attributed to the

spreading and accumulation resistance which is located mainly under the gate. It is noted, however, that the steepness does not alter the total R_S dramatically. The values range between 280 and 420 Ωμm. The variation in the current is also influenced by the L_{eff}, which is longer if the ratio R increases. This can be seen especially around V_T where the Rs has little influence. Here, the slope is smaller due to a larger L_{eff}.

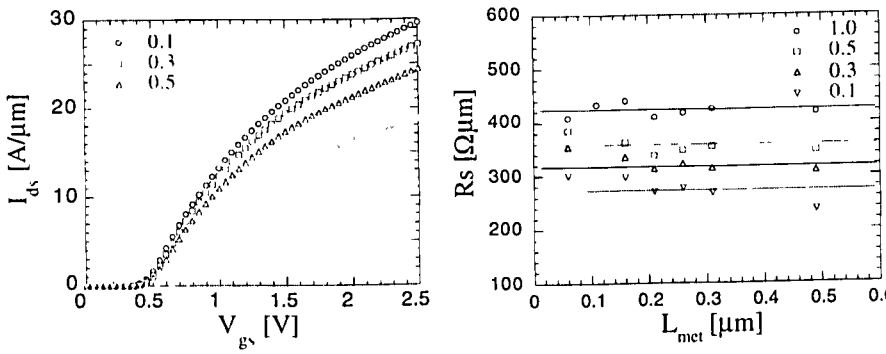

Fig.5 (left) I_{ds}-V_{gs} curve for Vds=20 mV and various values for R, (right) extracted R_S for the four different profiles under study

Depending on the specific requirements of the device, this study shows again the well known trade-off between SCE and performance, but includes the effect of the lateral S/D profile. This study allows to find out what the optimum steepness of this profile is to comply with a given set of specifications on the saturation and leakage current. It is clear that a steep profile has the highest I_{sat} but also suffers most from SCE. An optimum can be found. It is then up to the process engineer to find out how this profile can actually be fabricated.

References

[1] S. Biesemans, K. De Meyer, proceedings SISPAD, p.46 , 1996

[2] S. Biesemans, S. Kubicek, K. De Meyer, Symposium VLSI Technology, p.166, 1996

[3] S. Biesemans, A. Nackaerts, "m-S&R", demo software package for MAC and PC

[4] S. Kubicek, S. Biesemans, K. De Meyer, Symposium VLSI Technology, p.105, 1995

[5] K.K. Ng, W. T. Lynch, IEEE Trans. on Electron Devices, p.965, July 1986