Two-dimensional Device Simulator for Cyclic Bias Application

Yasuo Ohno and Yuji Takahashi
Optoelectronics Research Laboratories
NEC Corporation
Tsukuba, Ibaraki, Japan

Abstract — A two-dimensional device simulator has been developed which searches for steady-states in cyclic bias applications. An conventional time domain device simulator calculates one period of the cyclic bias and the newly developed module finds a set of internal device parameters which gives the same values at the beginning and at the end of the unit cycle. The simulator is applied to the analysis of pulse pattern effect due to deep traps in GaAs heterojunction FETs on semi-insulating substrates.

I. INTRODUCTION

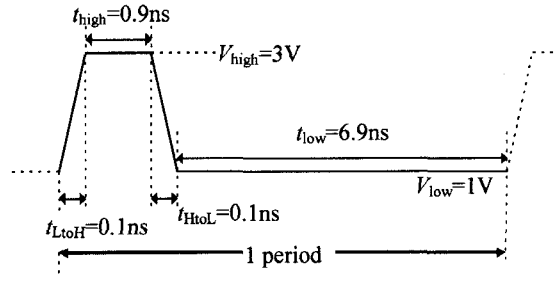
Semiconductor device simulators have been used for determining physical parameters, for designing device structures ,and also for trouble shooting in products. In these applications, comparison with experiments is the most important issues. Simulator users always require simulators with high accuracy, and measurements should be accurate as well. The DC characteristics of devices can easily be measured, but unlike the output of device simulators and circuit simulators, transient performances are always difficult to measure. Device dynamic performance is normally characterized by responses to periodic signals such as sinusoidal waves for microwave devices and train of pulse signals for digital ICs. The reason is that repetitive measurements can easily extract real signals from background noises, can cancel accidental noises, and can make it easy for impedance matching in measurement systems by limiting the frequency ranges. In periodic bias measurements data are read at a steady state. The time to reach the steady state may be long enough even for slow responses in the devices.

Conventional semiconductor device simulators calculate steady-states (DC), time sequence or small signal cases. Time domain simulators can be used for periodic signals by successively applying unit signals, but the cycle numbers to reach steady state may be extremely long if the device contains slow phenomena like deep traps in GaAs, or floating substrates in SOI. We developed a device simulator that elaborately calculates the device performances under periodic bias conditions. In this paper we report the algorithm and structure of the simulator. Then, an example of the application is shown for high-speed GaAs digital circuit devices, where very slow deep level reaction causes degradation of the high-speed performance of the digital circuits.

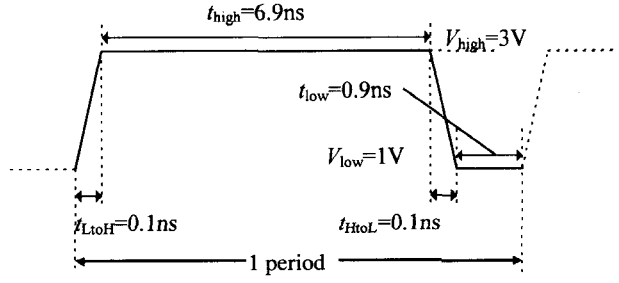
II. SIMULATOR STRUCTURE

Examples of periodic signals are shown in Fig. 1. Figure 1(a) shows a unit of a 1 Gbps NRZ (non-return to zero) signal with a mark ratio (the ratios of high level pulse numbers) of 1/8. The signal starts at 1 V at $t = 0$ ns, linearly increases to 3 V for 0.1 ns, stays at 3 V for 0.9 ns, decreases to 1 V for 0.1 ns and stays at 1 V for 6.9 ns. The total period is 8 ns. For 1/8 of the period, the signal is higher than the center voltage of 2 V.

When such bias is applied to the drain of an FET which has been in the steady state at the drain voltage of 1 V, the internal state parameters such as electric potential and carrier concentrations start to vary as the drain voltage changes. The state parameters after the unit cycle, however, will almost be back to the initial values, because the electrode voltages have returned to the starting values. When the unit sequences are applied repeatedly, the state parameters at certain time of the pulse, say $t = 0$ ns, will slightly change and finally they converge to values.



(a) Pattern A. Mark ratio = 1/8



(b) Pattern B. Mark ratio = 7/8

Fig. 1 Units of cyclic signals. One bit is 1ns long and non-return to zero (NRZ) between the bits.

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The steady state condition under a periodic bias application is defined as that where all the internal and external parameters of the device are invariant for the application of a single cycle of periodic bias. The calculations for the single step can be done with conventional time domain simulators. It is therefore necessary to make a step to find the set of parameters which will give no variation after a single period of the cycle. We used an existing device simulator for the single period calculation. The simulator solves the electron continuity equation, the hole continuity equation, and Poisson's equation with drift-diffusion transport expressions in two-dimension by using a finite element method. It comprises the SRH statistics model for deep traps in Poisson's equation and in generation-recombination process.

The core module calculates one period of the bias cycle starting with a set of state parameters for all the mesh points in the devices. Taking X as one of the parameters at one of the mesh points, and starting with X_k^I at k-th loop, X may become X_k^F at the end of the cycle. We define the variation d_k at k-th external loop as, $d_k = X_k^F - X_k^I$. The goal is to find the set of X's which make all the $d = 0$. The external loop, as shown in Fig. 2, searches for the solution. We used linear extrapolation or interpolation to predict new Xs as,

$$X_{k+1} = X_k - \frac{\gamma d_k}{d_k - d_{k-1}}(X_k - X_{k-1}), \qquad (1)$$

where γ is a dynamic relaxation coefficient introduced to keep new Xs not far from the previous values.

The state parameters which define the internal state of the device will be electrostatic potential ψ, electron concentration n, hole concentration p and trap electron occupancies f_T. In the present simulator, the carrier drift mobility model is a function of the current value. Therefore,

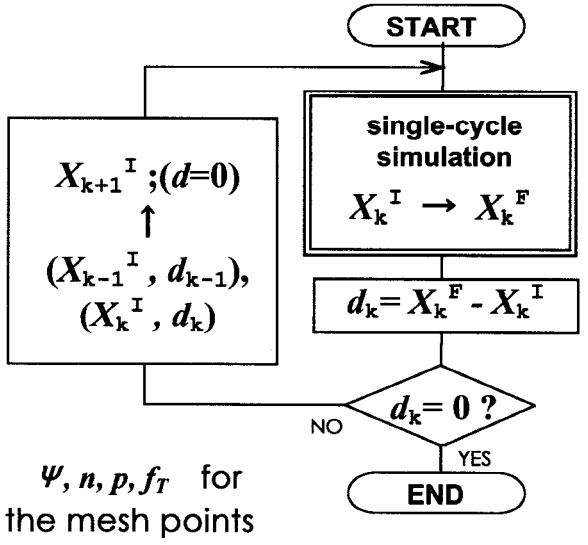

Fig. 2 Structure of the cyclic-bias simulator. A conventional simulation module is used for the calculation for single-cycle.

the mobilities are implicit functions of the state values. We also included local mobility values as the internal parameters.

To avoid carrier concentrations of negative values and an f_T not between 0 and 1, quasi-fermi levels for these values were used as shown in Table 1. Convergence criteria are defined as $\Sigma(\Delta\chi)^2/\Sigma\chi^2 < 10^{-10}$, where χs are ψ and quasi-fermi levels for n, p and f_T's. Drift mobility is omitted from the convergence evaluation.

Since the estimations are independent among these parameters and mesh points, the estimated values may not satisfy the basic physics law before they reach the convergence. This can commonly happen in conventional device simulations in initial condition setting and was not a problem.

Two sets of starting values are needed for the first estimation. We used a steady state solution for two extreme values of the periodic bias. First we calculate the DC solutions for the two biases. Then, the solutions were relaxed to the bias condition at $t = 0$ ns with a relaxation time corresponding to the unit cycle time. When the convergence is obtained, the final iteration results are stored in file for the output and other post processing.

Ⅲ. APPLICATION TO PULSE PATTERN EFFECT ANALYSIS IN GaAs FET

We applied this simulator to analyze the "pulse pattern effect" of a heterojunction FET made on a semi-insulating GaAs substrate. The effect is one of the most serious problems for high-speed digital ICs. Signal transition time from low to high or high to low in logic circuits depending on the signal mark ratio. These effects are attributed to deep traps in the semi-insulating substrate [1]. When these effects happen, signal eye diagram opening shrinks and noise margin decreases. For high-speed digital applications such as in 10 Gbps transmission systems, this effect will be fatal.

The device structure used in the simulation is shown in

Table 1. Internal device parameters used in the simulator

State Parameter	Symbol	Value used in calculation
electrostatic potential	ϕ	ϕ
electron concentration	n	$kT\ln\left(\frac{n}{N_C}\right)$
hole concentration	p	$kT\ln\left(\frac{p}{N_V}\right)$
drift mobility	μ_n, μ_p	μ_n, μ_p
trap occupation	f_T	$kT\ln\left(\frac{1-f_T}{f_T}\right)$

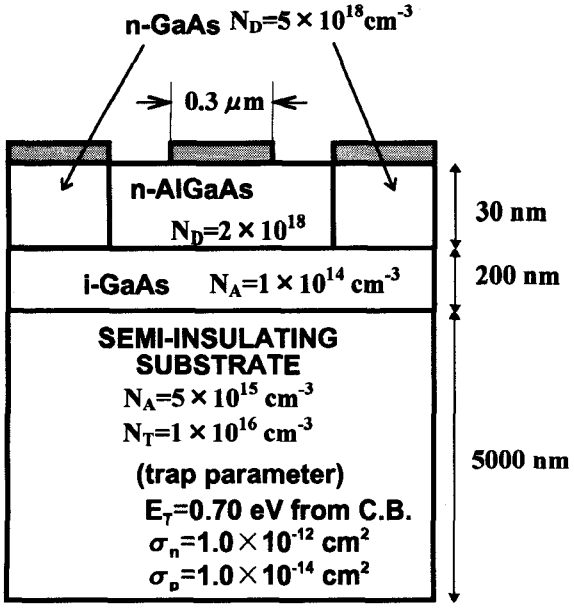

Fig. 3 Heterojunction FET structure for the test simulation. Channel transit time is about 10 ps, whereas the trap emission time is about 30 ms, $3x10^6$ times difference of time constants exists in the structure.

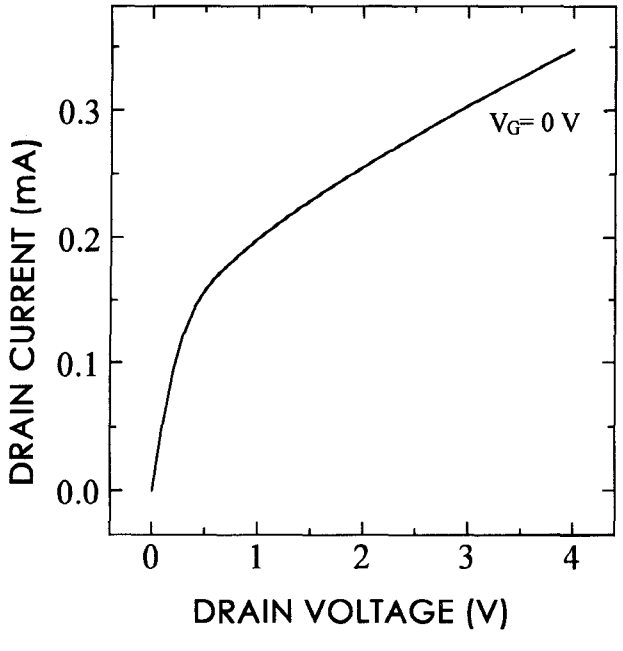

Fig. 4 DC I-V characteristics of the HJFET. The channel width is 1 μ m.

Fig. 3. A 200 nm thick channel i-GaAs layer was placed on a 5 μm thick semi-insulating substrate. The substrate contains $1x10^{16}cm^{-3}$ deep electron traps with compensating shallow acceptors. The electron emission time is 29.3 ms and the hole emission time is 9.89 sec. When a bias is applied, the device will reach the steady state after around these periods.

Measurements of high-speed digital ICs are normally

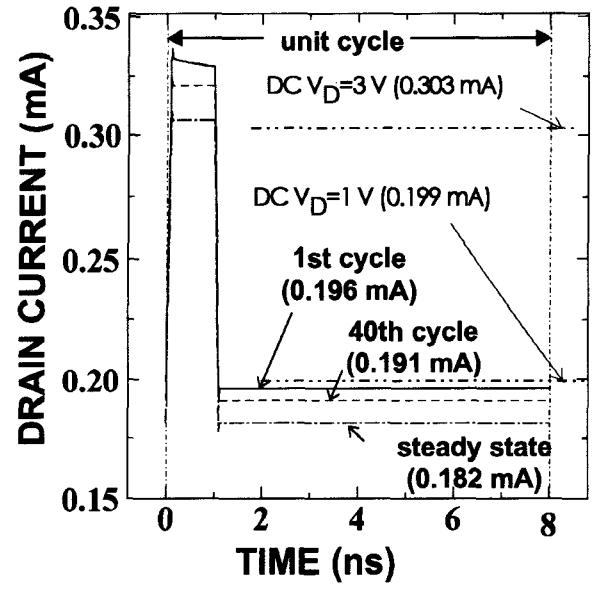

Fig. 5 Drain current profiles for various times after the application of a pulse-pattern cycle. The pulse pattern was a 1 Gbps NRZ signal of 1/8 mark ratio. Current level decreases until electron capture in the trap at V_D=3V for 1 ns is equal to electron emission at V_D=1V for 7 ns.

carried out using 2^{15}-1 bit long pseudo-random pulses with average mark ratio as 1/8, 1/4, and 3/8, etc. The cycle length seems to be long but it is only 30 μ s in case of 1 Gbps signal. Since the period is short enough for deep traps, the effect can be analyzed using simple 8 bit pulses as shown in Fig. 1. We applied the pulse voltage to the drain terminal while the source and gate voltage were kept constant.

Figure 4 shows the DC I-V characteristics of the FET. Figure 5 shows the conventional transient simulation results when the pulse signal was repeatedly applied. The figure shows the first cycle and the 40th cycle responses. The steady state solution obtained with the cyclic bias simulator is also shown. The current level gradually decreases as the cycle number increases. This is the result of electron capture by the traps. The electron concentration in the trap region increases from that at V_D = 1 V when the 3 V drain voltage is applied. The traps will capture electrons, but a single pulse width is too short to reach steady states. As the pulse signals are successively applied, the captured electron number increases. Then the emission of electrons from the traps also increases. In the steady state, the capture at V_D = 3 V period and the emission at V_D = 1 V period balance. Figure 6 shows the variation of the low-level drain current up to 200 pulses. The figure shows the exponential decrease in the current. From the figure, the cycle number to reach the steady state is estimated to be 50,000. The number corresponds to the duration of 0.4ms.

Figure 7 compares for the pulses with the mark ratio of 1/8 and 7/8. The current levels are slightly different. If this happens in a SCFL circuit, the switching threshold level moves due to the imbalance of FET currents in the

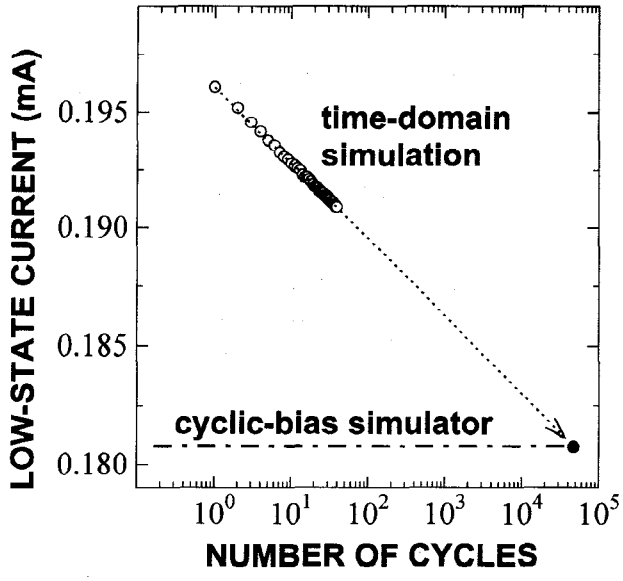

Fig. 6 Low-state current in the pulse as a function of the number of cycles in time-domain simulation. From 40 cycles of time-domain calculations, the extrapolated number of cycles to reach the steady state was about 40000 calculation cycles. This number corresponds to 0.3 ms of real time, extremely short time for the measurement setup.

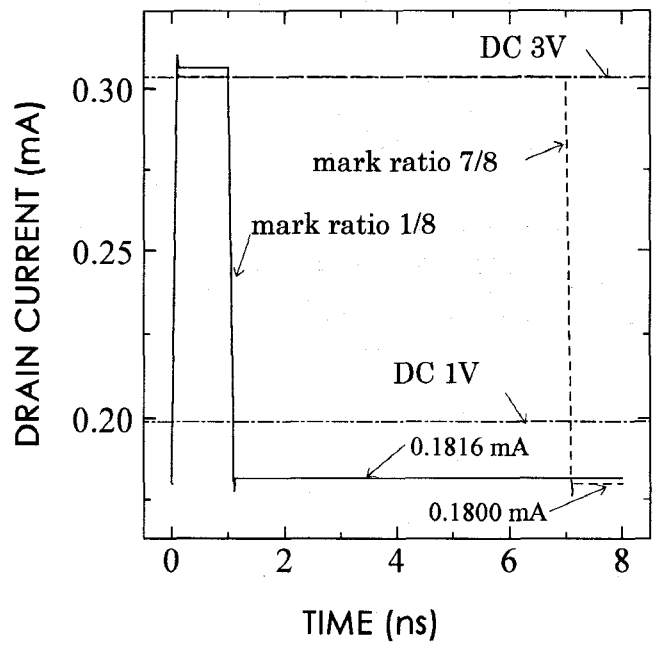

Fig. 7 Drain current profiles for 1Gbps NRZ signal with mark ratio 1/8 and 7/8, respectively. V_G=0V and drain biases are shown in Fig.1.

differential pair. The difference between signals with the mark ratios of 1/8 and 7/8 is relatively small (0.1816 mA and 0.1800 mA) compared with the DC current level (0.199 mA) in this case. For the present device structure and trap parameters, significant trap charge capture occurs at very low mark ratio and almost saturates at the mark ratio higher than 1/8.

IV. CONCLUSION

A two-dimensional device simulator which solves steady-states under cyclic bias application has been developed. An existing device simulator calculates the single period of the cycle and the newly developed module searches for a set of internal device parameters which give the same values at the beginning and the end of the unit cycle. The simulator was compared with conventional time domain simulator and confirmed that the simulator is effective for the analysis of devices with slow phenomena like deep traps. The simulator was used in the analysis of the pulse pattern effect of GaAs heterojunction FETs and obtained different current levels for different mark ratio of the applied pulses.

The simulator will especially be useful for the comparison with experimental results because high-speed devices are normally measured using cyclic bias conditions. Detailed analyses of troubles and parasitic phenomena related to deep traps can be carried out using this simulator on device structures and material parameters. Such analysis could only be done using circuit simulators by assuming circuit models previously. In addition, close comparison with experiments will make it possible to accurately evaluate the models and parameters used in the simulator. We believe that the present simulator extends the application area of device simulations.

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REFERENCES

[1] K. Kunihiro, M. Nogome, and Y. Ohno, "Effects of Buried p-Layers on Substrate-Trap Induced Phenomena in GaAs MESFETs," *Proc. 1995 GaAs IC Symposium*, p. 267 (1995)

[2] K. Kunihiro and Y. Ohno, "A Large-Signal Equivalent Circuit Model for Substrate-Induced Drain-Lag Phenomena in HJFET's," *IEEE Trans. on Electron Devices*, Vol. 43, p. 1336 (1996)