Accurate Models for CMOS Scaling and Gate Delay in Deep Sub-micron Regime

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Abstract

Accurate models for drain saturation current including velocity saturation, finite thickness of inversion layer due to quantization effect, mobility degradation due to vertical electrical field in the channel, and parasitic S/D series resistance, and their experimental confirmation with measurement data are presented. Furthermore, models for load capacitance and CMOS propagation delay are proposed and experimentally confirmed.

I. INTRODUCTION

CMOS device and speed projection for future technologies considering device and supply voltage scalings and interconnect loading have been dissatisfactory. This paper presents the accurate models for drain saturation current and propagation delay, all based on physical and process parameters such as V_{gs}, V_{th}, T_{ox}, L_{eff}, etc. Wafers with T_{ox} from 2.5 to 5.8nm were fabricated and characterized for the purpose of verification.

II. MODELS

Universal mobility model explicitly depending on gate bias (V_{gs}), threshold voltage (V_{th}) and gate oxide thickness (T_{ox}), has been developed [1]. The universality for both NMOS electrons and PMOS holes are shown in Fig. 1.

Given the physical parameters V_{gs}, V_{th}, and T_{ox}, mobility of both N- and P-MOSFETs can be accurately predicted by the empirical universal mobility model.

NMOS drain saturation current, I_{dsat}, considering velocity saturation, $v_{sat}=8\times10^{6}$cm/s, mobility degradation due to vertical field, $\mu_{eff}(V_{gs}, V_{th}, T_{oxe})$, as shown in Fig. 1 and parasitic S/D series resistance, R_s, has been found to be expressed as follows [2]:

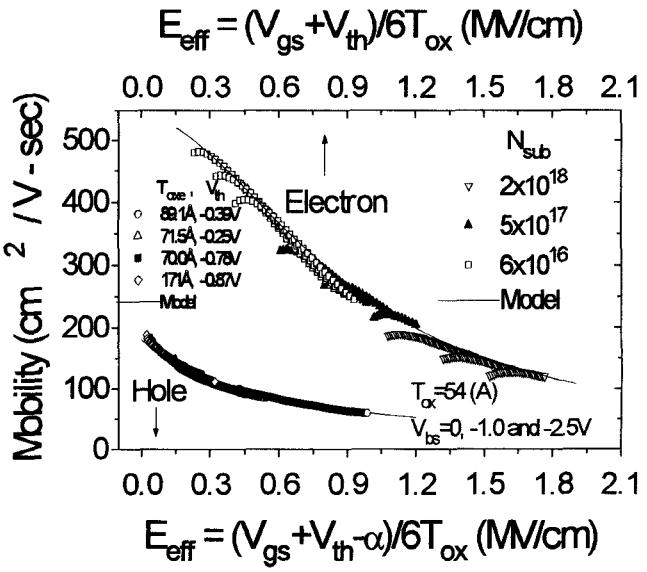

Fig. 1 Universal mobility model for both types of carriers solely dependent on V_{gs}, V_{th} and T_{oxe}.

$$I_{dsat} = I_{dsato} \Big/ \left(1+\frac{2I_{dsato}R_s}{V_{gs}-V_{th}}-\frac{I_{dsato}R_s}{V_{gs}-V_{th}+E_{sat}L_{eff}}\right) \quad (1)$$

where I_{dsato} is the drain saturation current when R_s=0:

$$I_{dsato} = \frac{W_{eff}\mu_{eff}C_{ox}}{2L_{eff}} \frac{(V_{gs}-V_{th})^2}{1+(V_{gs}-V_{th})/\frac{2v_{sat}}{\mu_{eff}}L_{eff}} \quad (2)$$

$E_{sat}=v_{sat}/\mu_{eff}$ is the lateral field where carrier's velocity saturates. Analytical equation of μ_{eff} can be found in reference [1].

For the deep sub-micron MOSFETs with very thin gate oxide (< 6nm), finite thickness of inversion layer due to quantum effect can not be ignored. It shows that electrically measured T_{ox} in strong inversion is consistently 0.4~0.7nm larger than the real physical T_{ox}. To account for these

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effects, electrically measured thickness, T_{oxe}, instead of physical thickness, T_{ox}, needs to be used in equations (1) and (2), as shown by the measurement data listed in Table 1 below.

TABLE 1
T_{ox} CHARACTERIZATION.

Measurement Methods	Gate Oxide Thickness (nm)			
Process target	2.5	3.5	4.5	6.0
Optical	2.5	3.6	4.7	5.8
Physical*	2.5	3.6	4.5	5.6
Electrical (C-V)	2.9	4.2	5.2	6.5

* Fowler-Nordheim tunneling current method.

The comparison of the prediction of the new I_{dsat} model and measurement data for wide range of V_{dd} and T_{oxe} is shown in Fig. 2. Based on the accurate model, future I_{dsat} with voltage, channel length and gate oxide scalings have been predicted as shown in Fig. 3. It shows that I_{dsat} will remain approximately

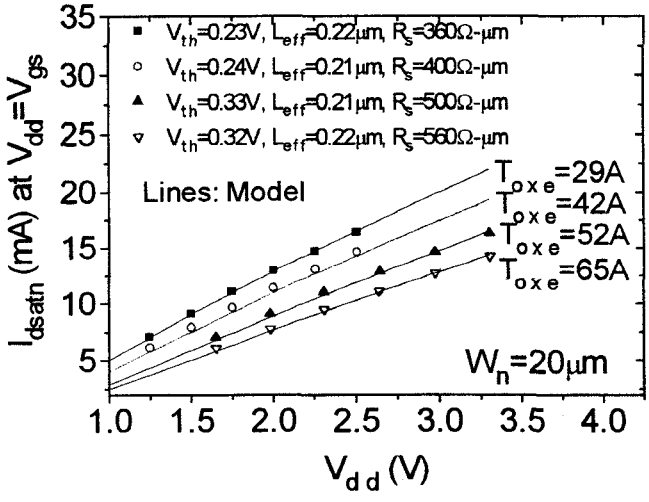

Fig. 2 The I_{dsat} model fits the measurement data well for wide ranges of T_{oxe} and V_{dd}.

at the range of 0.55-0.65 mA/μm.

The load capacitance, C_L, of CMOS ring oscillators, is modeled in the following way:

$$C_L = C_1 + A/C_{ox} \quad (3)$$

where C_1 represents the junction and interconnect capacitances and A/C_{ox} represents the T_{ox} related capacitance.

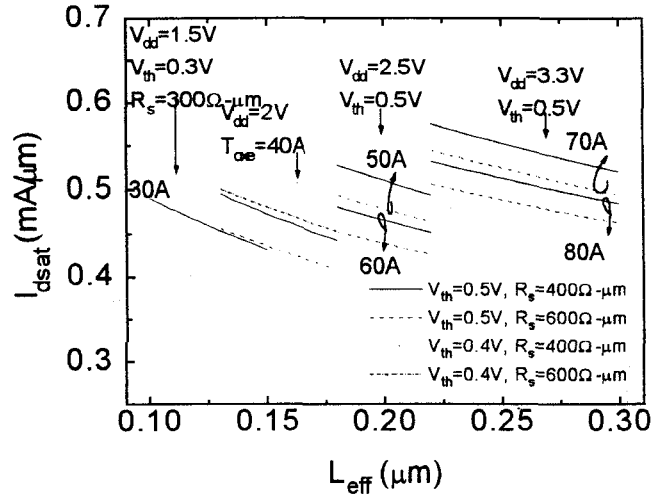

Fig. 3 Simulation results from the new I_{dsat} model shows that saturation currents for future technologies.

The propagation delay, t_{pd}, of CMOS ring oscillators can be expressed as follows [3]:

$$t_{pd} = \frac{C_L V_{dd}}{3.73}\left(\frac{1}{I_{dsatn}} + \frac{1}{I_{dsatp}}\right) \quad (4)$$

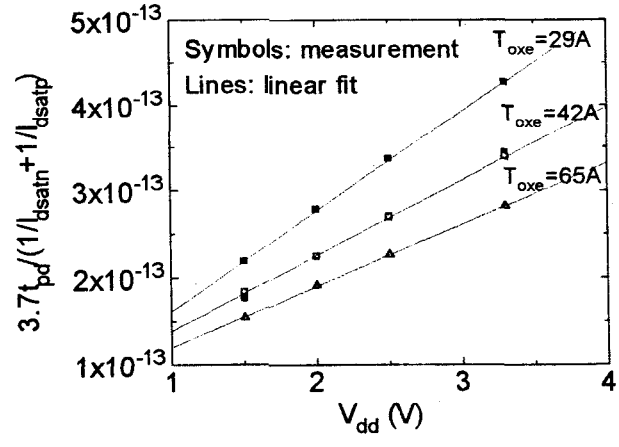

Fig. 4 a) Measuring t_{pd}, I_{dsatn} and I_{dsatp} in equation (1) can determine C_L (the slopes) for each T_{oxe}.

where V_{dd} is the power supply voltage and I_{dsatn} and I_{dsatp} are drain saturation currents for N- and P-MOSFETs, respectively.

Two independent methods to experimentally characterize C_L have been developed. The first method, a "DC" method, is to measure I_{dsatn}, I_{dsatp} and t_{pd} for different T_{oxe}. Based on equation (4), $3.73 t_{pd} / \left(\frac{1}{I_{dsatn}} + \frac{1}{I_{dsatp}} \right)$ is plotted as a function of V_{dd}. The slope of such a plot is C_L, as shown in Fig. 4 a). According to equation (3), if such determined C_L is plotted against $1/T_{oxe}$, constants "C_1" and "A" can be determined, as shown in Fig. 4 b).

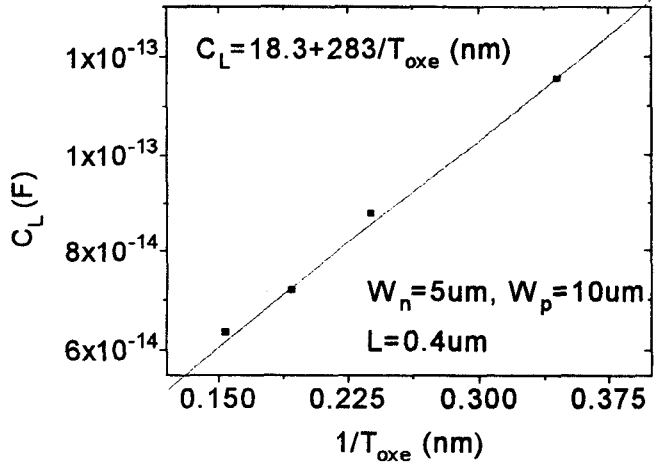

Fig. 4 b) Plotting C_L vs. $1/T_{oxe}$ obtained from Fig. 3 a) yields the values of C_1 and A in $C_L=C_1+A/T_{oxe}$.

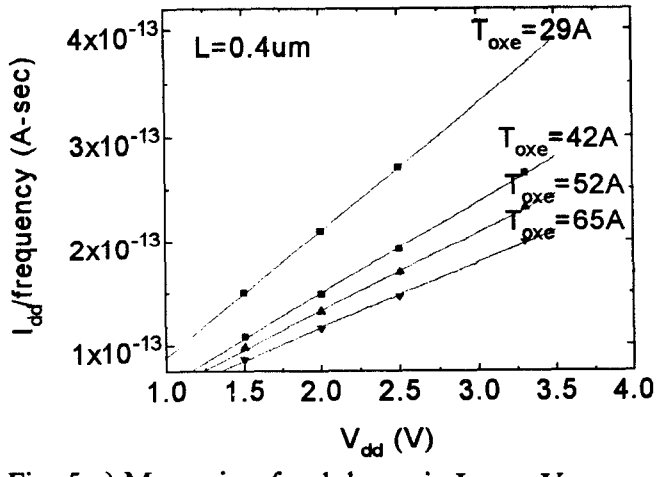

Fig. 5 a) Measuring f and dynamic I_{dd} vs. V_{dd} can get C_L for each respective T_{oxe} according to (7).

The other method, the dynamic current method, employs the following equation relating dynamic current between power supply and ground to operating frequency, f:

$$I_{cc} = fC_L V_{dd} = f(C_1 + A/T_{oxe})V_{dd} \qquad (5)$$

where f can be measured for ring oscillators. If I_{dd}/f is plotted against V_{dd}, C_L can be determined from the slope of each curve corresponding to each respective T_{ox}, as shown in Fig. 5 a). Similarly if C_L is plotted against its corresponding T_{oxe}, "C_1" and "A" in equation (3) can be determined, as shown in Fig. 5 b). As a matter of fact, both methods achieved the same result:

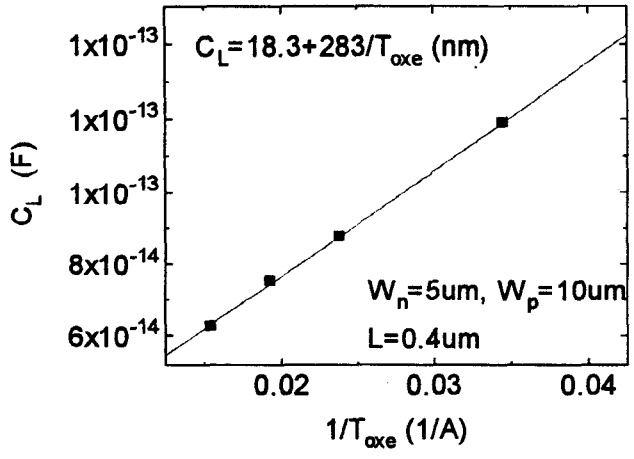

Fig. 5 b) Plotting C_L vs. $1/T_{oxe}$ obtained from Fig. 4 a) yields the values of C_1 and A in $C_L=C_1+A/T_{oxe}$.

$C_L(fF)=18.3+293/T_{oxe}(nm)$, for the particular ring oscillators fabricated.

To verify the t_{pd} model expressed in equation (4), CMOS devices and ring oscillators with 2.5 to 5.7 nm T_{ox} and minimum L_{eff}=0.22μm were fabricated.

t_{pd} can be projected from equations (1) through (4). Fig. 6 shows the comparison between the predicted t_{pd} and the measurement data for wide ranges of T_{oxe} and V_{dd}. The cross-overs in the figure indicate that optimum T_{oxe} exist because of competition between increased I_{dsat} (discounted by mobility degradation due to vertical field and velocity saturation due to lateral field) and increased C_L with decreasing T_{oxe}.

The impact of interconnect loading on CMOS speed can be modeled as well. Fig. 7 shows the projected t_{pd} as a function of interconnect loading. When C_{int} is increased, the corresponding optimum

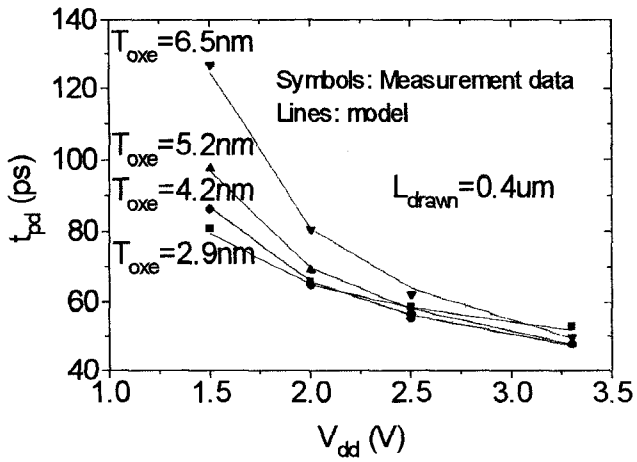

Fig. 6 t_{pd} vs. V_{dd}: model fits measurement data well for wide ranges of T_{oxe} and V_{dd}.

T_{oxe} is smaller and the window also becomes narrower. More attention should be paid in picking T_{oxe} for circuits with heavier loading.

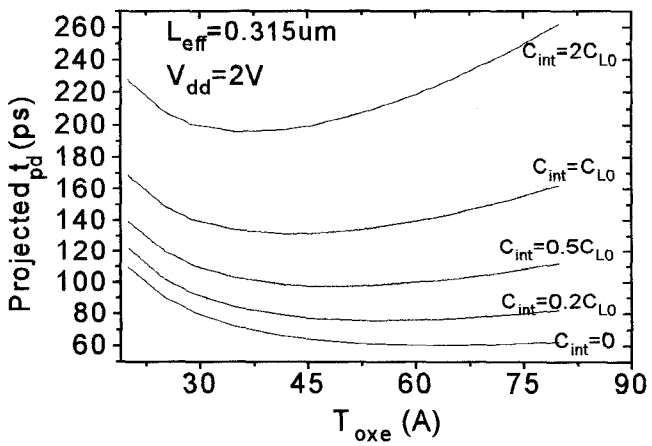

Fig. 7 Optimum T_{oxe} is smaller and the process window for optimum T_{oxe} is narrower for the heavier loaded circuits.

III. CONCLUSIONS

Knowing the physical and process parameters such as V_{th}, V_{gs}, R_s, and T_{oxe}, carrier mobility, I_{dsat}, t_{pd}, and optimum T_{ox} can be accurately predicted. The prediction has been verified with wide ranges of T_{ox}, L_{eff}, and V_{dd}. The successful development of these models offers an analytical tool that has been very much wanted but missing to study CMOS scaling and future IC performance in the first order.

IV. ACKNOWLEDGEMENT

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V. REFERENCES

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