Modeling Reverse Short Channel and Narrow Width Effects in Small Size MOSFET's for Circuit Simulation

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Abstract-- Modeling of small size MOSFETs and experimental verification of the model using devices with varying pocket implant processes are presented. The results show that the model can well describe reverse short channel and narrow width effects and match the measured characteristics of threshold voltage and saturation current over a wide range of channel lengths and widths down to 0.12um regime.

I. INTRODUCTION

Devices with pocket implant processes and different isolation technologies will play an important role in the production of future VLSI circuits. As a result, the circuit designers need an accurate model in circuit simulation to describe the electrical characteristics of MOSFETs, which have some particular characteristics, such as reverse short channel effect (ISCE) and/or reverse narrow width effect (RNWE) [1,2,3]. In this paper, we present the results on the modeling of short channel and narrow width effects with experimental verification in devices down to 0.12um.

II. MODELING

For devices with pocket implantation, the doping concentration Nch along the channel is not uniform, which causes the increase in threshold voltage (Vth) [4, 5]. This effects has been accounted for in an analytical Vth expression. Besides considering normal short channel and narrow width effect, this Vth model has also accounted for the ISCE and RNWE as well as small size effect in devices with *both* narrow width and small channel length to describe the Vth characteristics accurately. With all of the above considerations for lateral non-uniform channel doping, short channel, narrow width as well as small size effects on threshold voltage, the complete threshold voltage expression is given in (1):

$$\begin{aligned} V_{th} = {} & V_{tho} + K_1(\sqrt{\Psi_s - V_{bs}} - \sqrt{\Psi_s}) - K_2 V_{bs} + \\ & K_1\left(\sqrt{1+\frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\Psi_s} + \\ & (K_3 + K_{3b}V_{bs})\frac{T_{ox}}{W_{eff} + W_0}\Psi_s \\ & - D_{VT0w}[\exp(-D_{VT1w}\frac{L_{eff}}{2l_{tw}}) + \\ & 2\exp(-D_{VT1w}\frac{L_{eff}}{l_{tw}})](V_{bi} - \Psi_s) \\ & - D_{VT0}[\exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + \\ & 2\exp(-D_{VT1}\frac{L_{eff}}{l_t})](V_{bi} - \Psi_s) \\ & - [\exp(-D_{sub}\frac{L_{eff}}{2l_{to}}) + 2\exp(-D_{sub}\frac{L_{eff}}{l_{to}})] \\ & (E_{ta0} + E_{tab}V_{bs})V_{ds} \end{aligned} \quad (1)$$

Where V_{tho} is the threshold voltage for a long channel device, T_{ox} is the thickness of gate oxide, Ψ_s is $2\Psi_b$, and is given by $2v_t \ln(\frac{N_{ch}}{n_i})$, V_{bi} is the built-in potential of drain/source-body junction, l_t and l_{tw} are functions of T_{ox} [6]. Channel doping concentration and body bias. K_1, K_2, D_{VT0}, D_{VT1}, D_{VT0w}, D_{VT1w}, D_{sub}, E_{ta0}, E_{tab}, W_0,

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K_3, K_{3b} and N_{lx} are parameters to be extracted from the measured data.

The effective channel length and width are two important parameters in the circuit design, especially for very small size devices. It has been found that the values of dL and dW, parameters describing the effective channel length and width, can be very different between the devices with small sizes and large sizes. The geometrical dependence of dL and dW has been included in the model to simulate deep sub-quarter micron devices accurately. Furthermore, the gate and body bias dependence of dW has also been accounted for in the model.

The effective channel length and width are given by:

$$L_{eff} = L - 2dL \quad (2)$$

$$W_{eff} = W - 2dW \quad (3)$$

$$dL = L_{\text{int}} + \frac{L_l}{L^{Lln}} + \frac{L_w}{W^{Lwn}} + \frac{L_{wl}}{L^{Lln} W^{Lwn}} \quad (4)$$

$$dW = W_{\text{int}} + dW_g(V_{gs} - V_{th}) + dW_b(\sqrt{\psi_s - V_{bs}} - \sqrt{\psi_s}) + \frac{W_l}{L^{Wln}} + \frac{W_w}{W^{Wwn}} + \frac{W_{wl}}{L^{Wln} W^{Wwn}} \quad (5)$$

where W_{int}, dW_g, dW_b, W_l, W_w, W_{ln}, W_{wn}, W_{wl}, L_{int}, L_l, L_w, L_{ln}, L_{wn} and L_{wl} are extractable parameters.

Another important parameter in modeling very small size devices is drain/source parasitic resistance Rds. Because of the existence of the LDD regions, the series resistances can be modulated significantly by the gate and body biases. An effective Rds expression considering influnce of gate and bosy bias has been used in this paper [7]:

$$R_{ds} = \frac{R_{dsw}[1 + P_{r\,wg}(V_{gs} - V_{th}) + P_{r\,wb}(\sqrt{\psi_s - V_{bs}} - \sqrt{\psi_s})]}{W_{eff}'^{\,W_r}} \quad (6)$$

Where W_{eff}' is the effective channel length ignoring the influence of gate and body biases, R_{dsw} is the resistance per unit width and can be extracted from the measured data together with the parameters W_r, P_{rwg} and P_{rwb}.

III. EXPERIMENTS

The devices used in this study are fabricated with three different technologies. Device A and B are n-MOSFETs with LDD and p-pocket implant LDD fabricated with a dual-gate CMOS process. The gate oxide thickness is 4nm. The condition of boron implantation in channel region is 30kev and $4x10^{12}cm^{-2}$ for device A, and 40kev and $8x10^{12}cm^{-2}$ for device B. The pockets were formed with a BF_2 implantation condition of 50kev and $2x10^{13}cm^{-2}$ for device A, and a B implantation condition of 10kev, $8x10^{12}$ cm^{-2} for device B. The n-LDD regions are formed by As^+ implantation (10kev, $2x10^{14}$ cm^{-2} for device A and 10kev,$4x10^{13}$ cm^{-2} for device B). The device geometry range is from 0.12um

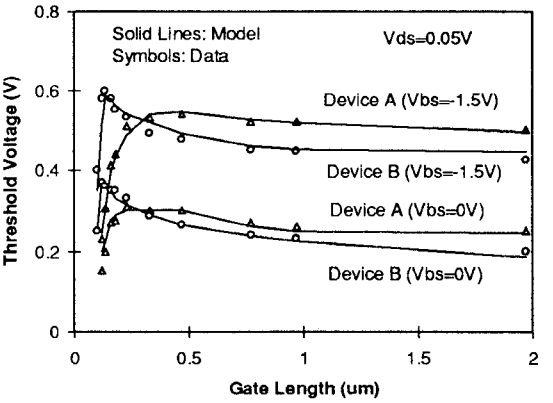

Fig. 1 Model and measured characteristics of threshold voltage vs. channel length at Vds=0.05V and different body bias conditions. The model can match the data well for the devices with different pocket process conditions.

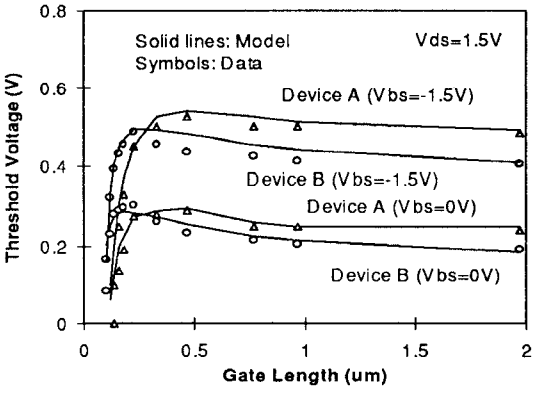

Fig. 2 Model and measured characteristics of threshold voltage vs. channel length at Vds=1.5V and different body bias conditions, for the devices with different pocket process conditions.

to10um for the length, and from 0.15um to 5um for the width. For device C, there is no pocket implant. The gate oxide thickness is 12nm. Channel length ranges from 0.4 to 10um and channel widths range from 0.4um to 5um.

Fig.1 shows the modeled and measured Vth vs. L for the devices with different pocket technologies (device A and B) at Vds=0.05V and different body bias conditions. It can be seen that the measured data has obvious reverse short channel effect, and can be well simulated by the model.

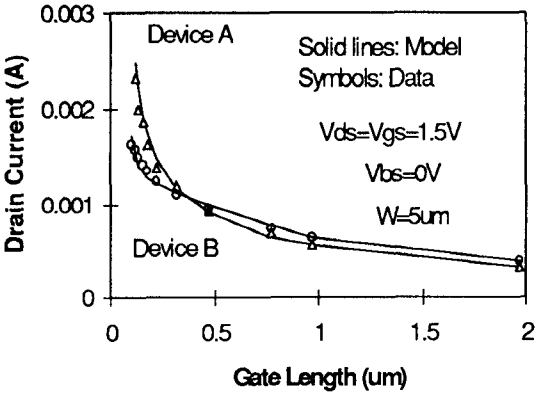

Fig.3 Model and measured characteristics of saturation current vs. channel length for the devices with different pocket process conditions.

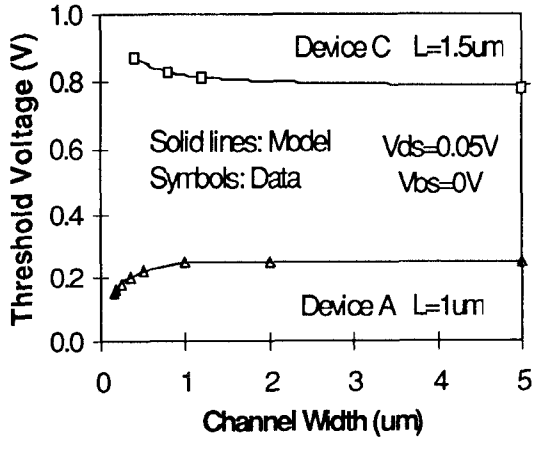

Fig.4 Model and measured characteristics of Vth vs. L for different isolation technologies.

Fig.2 gives also the measured and modeled Vth vs channel length but at Vds=1.5V and two different body bias conditions to show the model performance at high Vds. The same sets of parameters used in Fig.1 are used here. It demonstrates that the model can describe well the short channel effects including both DIBL and Vth roll-off for the devices at different conditions of channel engineering.

Fig.3 shows the saturation current characteristics of devices with different pocket technologies at Vgs=Vds=1.5V and Vbs=0V. Because the threshold voltage and saturation current are two very important parameters to predict the device performance in both digital and analog circuit design as well as statistical modeling, the results shown in this paper demonstrate that the model can be used in practical circuit design for the devices of channel length down to deep sub-quarter micron range.

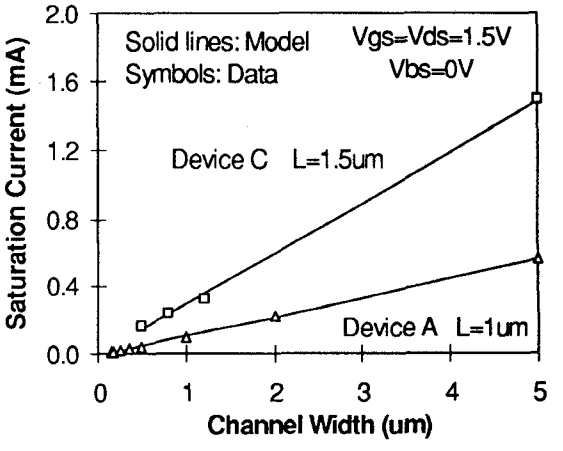

Fig.5 Model and measured characteristics of Idsat vs. L for different isolation technologies.

The modeled and measured Vth characteristics of device A at different channel widths are given in Fig. 4. It can be seen that the devices show strong reverse narrow width effect, and the model can match the measured data well for the devices of channel widths down to 0.15um. For comparison, we also exhibit the Vth characteristics of device C that shows normal narrow width effect. It can be

seen in Fig. 4 that both the normal and reverse narrow width effects can be simulated accurately by the model.

Fig. 5 shows the modeled and measured saturation current characteristics of device A and C with different channel widths. The model can match the measured data well for the devices with both normal and reverse narrow width effects. Based on the work in this paper, an I-V model can be derived.

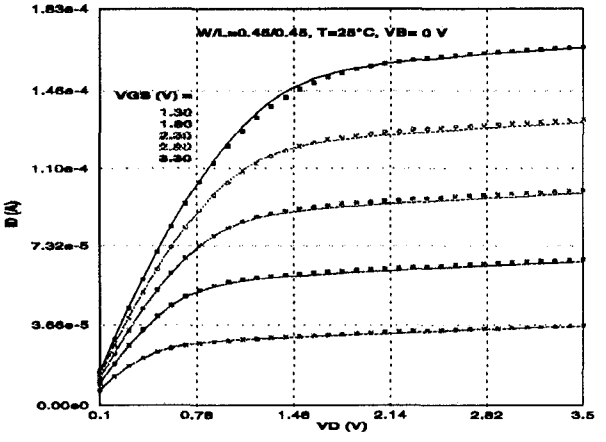

Fig.6 Model and measured Id-Vds characteristics of device C of W/L=0.45/0.45

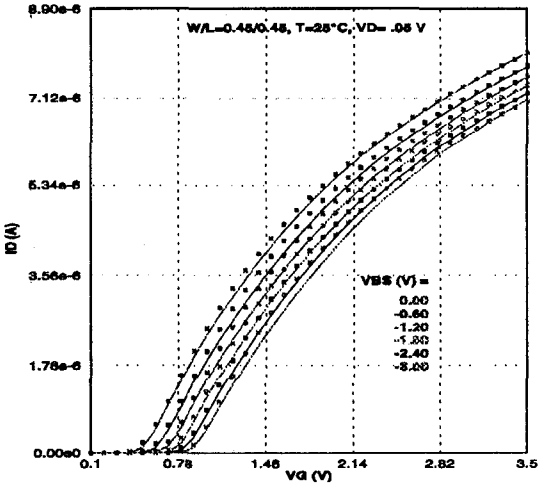

Fig.7 Model and measured Id-Vgs characteristics of device C of W/L=0.45/0.45.

Figs. 6 and 7 show the modeled and measured Id-Vds and Id-Vgs curves of the device C of W/L=0.45/0.45. It can be seen that the current charateristics of the small size device can be well simulated by the model.

IV SUMMARY

With the above results, we can summary that the model can describe well the reverse short channel effect for different pocket technologies, and is accurate for both Vth and current characteristics with Leff down to 0.12um. The model can also describe both the normal and reverse narrow width effect so that it can model the characteristics of devices with different isolation technologies.

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