Modeling of Saturation Velocity for Simulation of Deep Submicron nMOSFETs

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Abstract--The saturation velocity is one of the most important parameters for simulation of deep submicron nMOSFETs. The saturation velocity is modeled as a function of electron concentration by simulating the same structure as measured resistive gate MOSFETs. The saturation velocity lowering under the strong inversion condition is confirmed in single source/drain nMOSFETs. It is shown that the saturation velocity lowering effect and velocity overshoot effect are comparable in deep submicron nMOSFETs.

INTRODUCTION

In deep submicron MOSFETs, the high electric field region formed by drain bias has large occupancy in the channel length. In high electric field, carriers approach the saturation velocity v_{sat}. Consequently, v_{sat} is one of the most important physical parameters for prediction of the drain current Id's. While it has already been reported through the various techniques that v_{sat} in the inversion layer is lower than in bulk [1]-[3], the accurate v_{sat} model has not been established yet. The key issue in modeling v_{sat} is the separation of the effects of the velocity overshoot [4] and velocity lowering in the inversion layer.

In this study, the v_{sat} model, as a function of electron concentration, is established by analyzing RGMOS (Resistive Gate MOS), in which the velocity overshoot effect is eliminated experimentally. It is shown that high predictability of Id's can be achieved by using the present v_{sat} model together with ETM (Energy Transport Model).

v_{sat} MODELING BY RGMOS

In order to extract v_{sat}, the elimination of the velocity overshoot effect is necessary, which can be achieved by the uniform electric field distribution. We have reported the velocity vs. tangential field curves (Fig. 1) in the inversion layer by measuring RGMOS (inset in Fig. 1), with the surface electron concentration Ns, i.e. the gate voltage Vg as a parameter [1]. Vg1 and Vg2 are separately biased to make tangential field in the inversion layer uniform. By simulating the same device structure as used in [1], the saturation velocity as a function of electron concentration, $v_{sat}(n)$, can be modeled inversely as shown in Fig. 2.

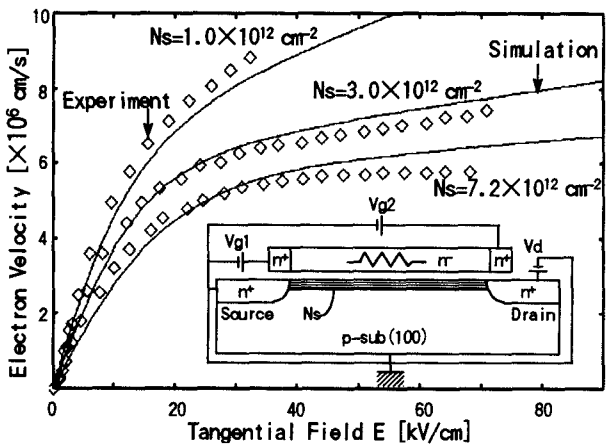

Fig. 1 Inset: schematic figure of RGMOS structure. Figure: plot of electron velocity vs. electric field, Ns as a parameter.

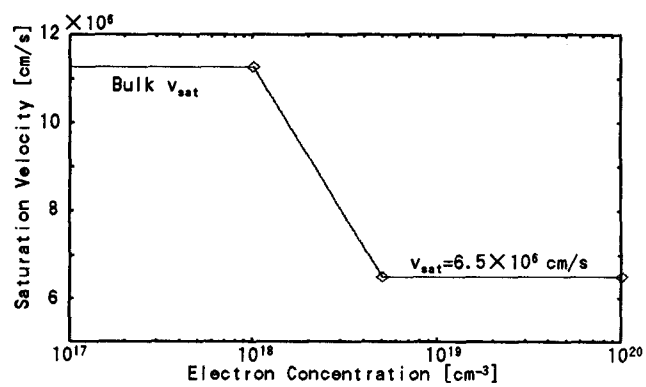

Fig. 2 Plot of newly introduced v_{sat} model as a function of electron concentration (n).

In the low electron concentration region (i.e. low gate voltage conditions), v_{sat} is the bulk value, and $v_{sat}=6.5\times10^6$ cm/s in the high electron concentration region (i.e. high gate voltage conditions). In this model, v_{sat} significantly decreases from the bulk value to 6.5×10^6 cm/s around $n=10^{18}$ cm^{-3}. Although the reason of lower v_{sat} in high concentration has not been fully clarified, the interaction between phonon and plasmon [1][5] may support the electron concentration dependence of v_{sat}, since the plasmon energy 40meV for $n=5\times10^{18}$ cm^{-3}, is close to intervalley phonon energy ranging from 12 to 60 meV, as shown in Fig. 3.

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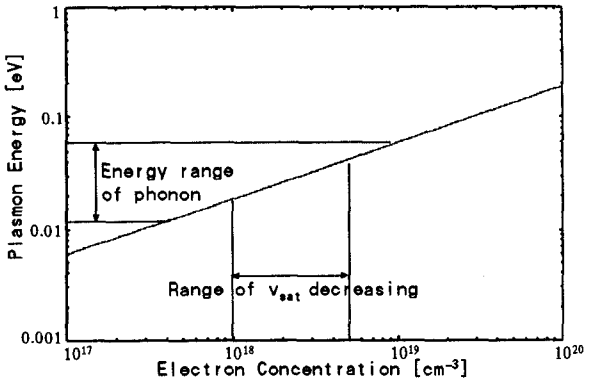

Fig. 3 Plot of plasmon energy vs. electron concentration.

v_{sat} LOWERING IN SINGLE S/D MOSFETs

In order to verify the v_{sat} lowering in the high electron concentration region, simulations are compared with measurements of usual nMOSFET structures, in which the uniform tangential field can only be formed under the high Vg voltage. Fig. 4 shows the tangential field distribution at the surface of the substrate under Vg of 15V in various gate lengths of single S/D nMOSFETs with n^+ poly silicon gate electrode, the surface impurity concentration of about 10^{17} cm^{-3}, the device width of 100 μm, and the gate oxide thickness tox is 200Å. The horizontal axis is normalized by the gate length. Sufficiently uniform field is obtained, in which the velocity overshoot effect is eliminated. Fig. 5 shows Id vs. the average tangential field given by Vd/L. Simulations with the bulk value of v_{sat} overestimate Id, while simulations with vsat=6.5×10^6 cm/s shows good agreement with measurements, which support v_{sat} lowering in the high electron concentration region.

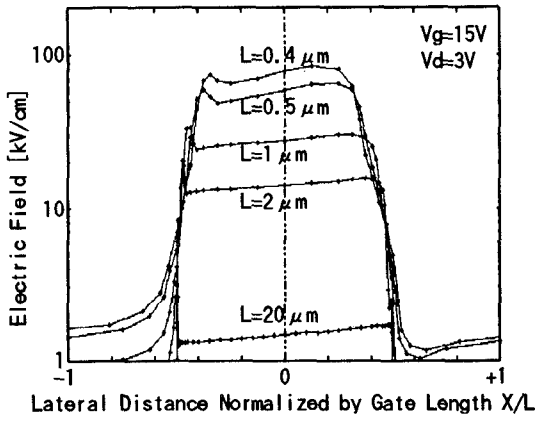

Fig. 4 Distribution of tangential electric field at the surface.

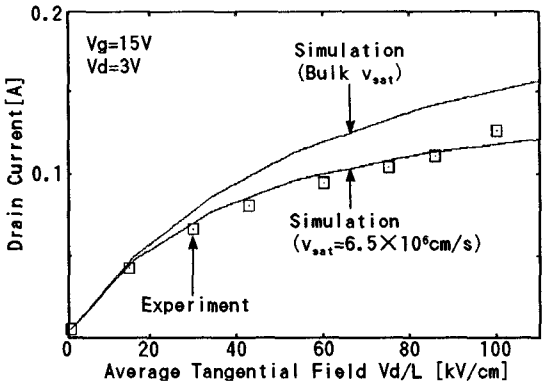

Fig. 5 Plot of Id vs. tangential electric field under high Vg (15V) showing the effect of v_{sat} value.

v_{sat} LOWERING AND VELOCITY OVERSHOOT EFFECTS ON DEEP SUBMICRON nMOSFETs

Simulations of ETM [6] with $v_{sat}(n)$ are performed for Leff=0.36 μm of single S/D nMOSFETs (solid line in Fig. 6), which reproduce the measured Id-Vg (symbols in Fig. 6). One important issue is that contributions of v_{sat} and velocity overshoot effect on Id's can be discussed qualitatively. As shown in Fig. 6, the v_{sat} lowering effect (deference between solid line and broken line) and the velocity overshoot effect (deference between solid line and two-dotted line) are comparable. Consequently, it is revealed that the evaluation of velocity overshoot effect assuming the bulk value of v_{sat} may have been underestimated.

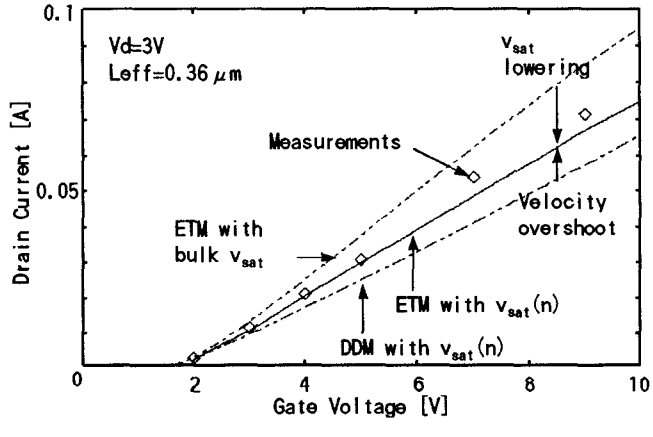

Fig. 6 Plot of Id vs. Vg of measurements, ETM with $v_{sat}(n)$, ETM with the bulk value of v_{sat}, and DDM with $v_{sat}(n)$.

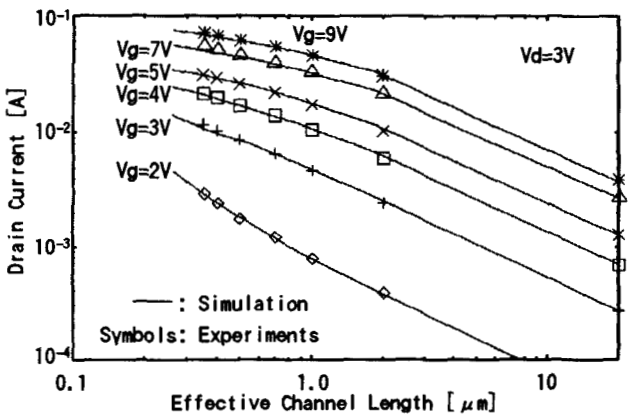

Fig. 7 Plot of Id vs. Leff for measurements and ETM with $v_{sat}(n)$, Vg as a parameter.

Finally, it is shown that simulated Id vs. Leff curves are in good agreement with measured results (Fig. 7). These results demonstrate that by introducing the present v_{sat} model and ETM, Id's for wide range of gate lengths and gate biases are reproduced successfully.

CONCLUSION

The saturation velocity in the inversion layer was modeled as a function of electron concentration by using RGMOS. By introducing the present v_{sat} model and ETM into the device simulation, high predictability of Id can be achieved for deep submicron nMOSFETs. It is pointed out that conventional simulations using the bulk value of v_{sat} underestimate the velocity overshoot effect.

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