2D Process and Device Simulation of Lateral and Vertical Si/SiGe High-Speed Devices

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Abstract--**Several adaptations to the properties of SiGe alloys, Si/SiGe heterojunctions and the implementation of all key processes and whole fabrication sequences to a 2D process simulator yield the estimation of the performance potential of novel high-speed device concepts by 2D physically based device simulation. For lateral L_G=0.15 µm SiGe MODFETs high drain currents around 450 mA/mm and transconductances up to 290 mS/mm have been calculated. Improved RF cut-off frequencies of f_{max}=120 GHz and f_t=55 GHz have been estimated for a given device structure in good agreement with experimental reference data. Reduced gate leakage currents and channel lengths below 100 nm are expected by the integration of vertical MOSFET devices. The incorporation of SiGe layers and hetero barriers minimizes the DIBL effect and thus reduces short-channel effects and off-state currents in vertical SiGe Hetero-MOSFETs.**

I. INTRODUCTION

Modern communication systems (e.g. mobile or satellite communication) require the development of novel Si-based high-speed transistors with low noise, improved current gain and reduced power consumption operating at frequencies in the GHz range. It is very expensive, time-consuming and practically impossible to base the development of design rules, fabrication processes and satisfactory transistor models on real experimentation. The combination of device and process simulation becomes inevitable, offering an opportunity to visualize physical phenomena which are not easily accessible to experimentation thus being able to proceed fast and effectively as well as to reduce the number of useless wafer batches.

The material system $Si_{1-x}Ge_x$ is, so far, the only heterosystem that is compatible with Si devices and circuits. The incorporation of Ge significantly changes the materials properties of the semiconductor layers thus offering the abilitity to combine the advantages of heterodevices with well-established Si technology.

In this contribution, the succesful implementation of high-speed devices, lateral SiGe MODFETs and vertical MOSFETs - one bare Si and a SiGe MOSFET - and the used models are described and confirmed by a very good agreement of simulated and experimental data.

II. IMPLEMENTATION

Empirical, usually one-dimensional, models to obtain analytic formulae provide efficient approximation and interpolation of characteristic device data, but they cannot provide insight to physical phenomena, which is absolutely necessary for the development of new heterodevice concepts.

A complete simulation of the whole process sequence is essential. The comprehensive capabilities of the used process simulators (e.g. SSuprem 4) including advanced oxidation, implantation and diffusion models as well as different deposition and etch models enable the simulation of complex geometries and MOS transistor structures. All the key processes e.g. lateral definition by mesa-etching, gate oxidation, poly silicon deposition, spacer etching, implantation and metallization have therefore been implemented in the SILVACO ATHENA process simulator [1] and adapted to the material system $Si_{1-x}Ge_x$. The resulting device structures were then used to calculate the electrical characteristics using the simulators ATLAS and BLAZE [1]. The physically based two-dimensional device simulators solve systems of the fundamental, coupled non-linear partial differential equations that describe semiconductor physics (i.e. Poisson equation, carrier continuity equation, charge transport) by an iterative method using finite elements methods.

The lattice constant of $Si_{1-x}Ge_x$ alloy layers differs considerably from that of bare Si and Ge. The addition of Ge to Si causes strain, modifies the energy band structure and reduces the band-gap of a $Si_{1-x}Ge_x$ layer. Calibration of the simulators is fundamentally necessary and requires an understanding of the software´s abilities in combination with an understanding of the underlying related physics. The adaptation of the simulators to the material system $Si_{1-x}Ge_x$ is inevitable. N-channel heterostructures with biaxially strained Si channel layers sandwiched between SiGe layers yield a splitting of the two-fold and four-fold degenerated conduction band levels. A type II band alignement with an

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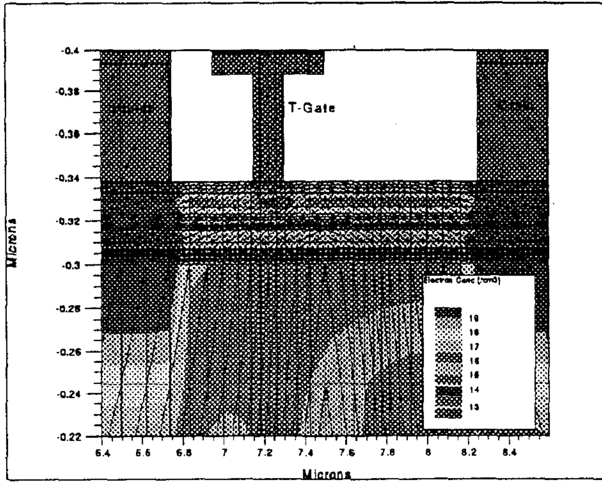

Fig. 1 Cross section of a 0.15 μm T-Gate SiGe n-MODFET after process simulation, the calculated free carrier distribution shows high carrier densisties in the channel and the contact zones.

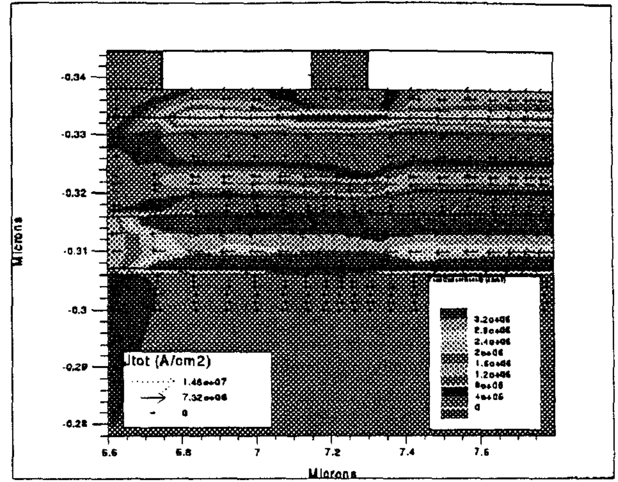

Fig. 2 The calculated current distribution in the SiGe MODFET structure at V_G=0.6 V and V_{ds}=3 V shows that current flow only occurs in the Si channel layer, spatially separated from the above and below situated n-doped SiGe supply layers.

abrupt hetero barrier which depends on strain and Ge-content and the formation of a 2DEG channel in the Si QW with considerably higher mobilities was taken into account. For the vertical Si and SiGe MOSFET structures standard and modified Si MOSFET models have been used, respectively.

The first step in simulation is to overlay an appropriate mesh. Mesh structures with variing grid size were used as a trade off between execution time and calculation accuracy. Regions where strong gradients of carrier concentration, potential and electric field are to be expected (e.g. beneath the gate, in contact zones, around channel and doping layers) were calculated with reduced grid size (see for example Fig. 1). The good agreement of calculated and experimental device characteristics described in the following confirms the validity of this approach.

III. RESULTS

A. Lateral SiGe MODFETs

Lateral SiGe MODFETs with in-plane current transport have shown impressive device performance because of the higher mobilities compared to bulk Si owing to the spatial separation of fixed ionized donors and free electrons in modulation-doped heterostructures and the thus significantly reduced Coulomb scattering. Fig. 1 shows a cross section of a 0.15 μm T-Gate SiGe n-MODFET structure after process simulation. The calculated carrier distribution that is included in the plot shows high carrier densities in the channel and in the ohmic source and drain contact zones which are realized by phosphorous implantation and rapid thermal annealing. A detailed description of the modulation-doped heterostructure layer sequence and the fabrication process is given in [2,3].

An enlarged cross section of thegate region is shown in Fig.2. A significant carrier confinement is observed in the two-dimensional electron gas (2DEG) channel, a 10 nm thick Si QW. As a consequence a high current flow in this Si channel layer sandwiched between SiGe layers and spatially separated from the n-doped supply layers, which are situated below and above the Si channel, is observed.

For all Hetero-FET structures, the most important transistor parameters like the transconductance (g_m), the cut-off frequency (f_t) and the maximum frequency of oscillation (f_{max}) are determined by extrinsic parasitic elements (mainly pad capacitances and resistances) and by the modulation efficiency as a measure of how effectively charges can be modulated beneath the gate. For these key parameters a trade-off in the doping concentration has to be found. Hetero-FETs often suffer from the formation of a parasitic MESFET in the doped layer especially under forward bias condition if the doping was chosen to high. The onset of such an unwanted parasitic channel can be seen in Fig. 2 and best be avoided using advanced 2D simulation. Figs. 3 and 4 show the calculated DC and RF characteristics. The higher current densities that have been calculated in comparison to experimental reference data point to some additional contact resistances. The estimated f_{max} and f_t data of up to 120 and 55 GHz, respectively, even at V_{ds}=1.5 V are only a bit higher than the reference data found from the used layer sequence (for further information see [3]) due to additional extrinsic parasitic resistances and variations in the lateral dimensions which are not completely included in the simulations. The high cut-off frequencies demonstrate the feasibility of this novel Si-based device generation especially for low power analog circuits design.

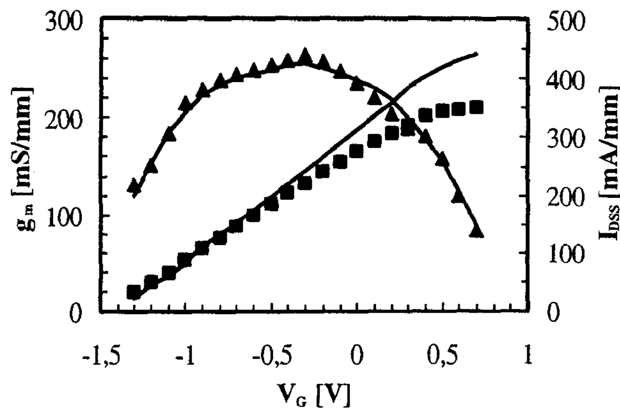

Fig. 3 Calculated and measured DC transfer characteristics (▲ g_m, ■ I_{DSS}) of a lateral L_G=0.15 µm SiGe MODFET as a function of gate voltage at V_{ds}=3 V.

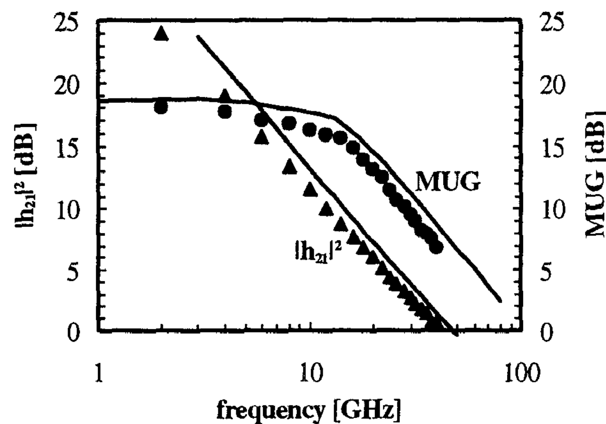

Fig. 4 Measured and calculated MUG (●) and $|h_{21}|^2$ (▲) versus frequency curves of a L_G=0.15 µm SiGe MODFET (V_G=0 V, V_{DS}=1.5 V, W_G=60 µm), f_t=43 GHz and f_{max}=92 GHz have been extrapolated from S-parameter measurements after parasitic elements extraction.

B. Vertical Si MOSFETs

Scaling limitations due to the minimum feature sizes that are achieved by state-of-the art lithography and problems with gate and off-state leakage currents can be overcome by vertical MOSFET structures (i.e. current transport perpendicular to the growth direction). The improved growth control in the nm range using e.g. molecular beam epitaxy (MBE) enables the realization of ultra-shallow doping profiles and channel lengths below 100 nm resulting in an improved device performance and packing density. Key challenges are the optimization of parasitic capacitances and series resistances and the control of short-channel effects.

Fig. 5 shows a schematic cross section of a vertical Si n-MOSFET. The layer stack consists of a several nm thick p-doped channel located between n^+ doped source and drain layers grown by molecular beam epitaxy (MBE). Respective p-channel MOSFETs consist of an n-doped channel

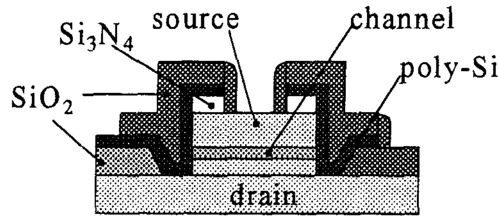

Fig. 5 Schematic cross section of a vertical Si MOSFET

positioned between p^+ doped source and drain layers. A detailed description of the fabrication process is given elsewhere [4].

The calculated and measured DC transfer (Fig. 6a) and output characteristics (Fig. 6b) are shown for 5x5 µm^2 vertical n-MOSFET with a $N_A=1\cdot10^{18}$ cm^{-3} p-doped L=200 nm channel and a 5 nm thick gate oxide which was formed in a wet high pressure oxidation step at 10^6 Pa and 600°C. A subthreshold slope of 105 mV/dec and a threshold voltage V_{th}=0.7 V was derived at $I_D(V_{th}=)=1\cdot10^{-7}$ A/µm. DC transconductances of 120 mS/mm are found at V_{ds}=-1.5 V in good agreement with simulation.

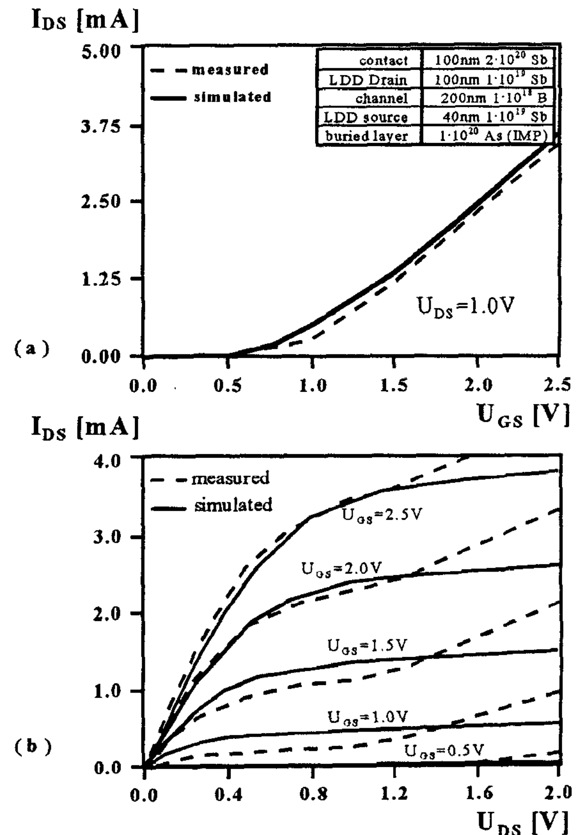

Fig. 6 Measured and calculated drain current as a function of gate voltage (a) and DC output characteristics (b) of a 5x5 µm^2 vertical MOSFET.

For corresponding p-MOSFETs (channel doping $N_D=1\cdot10^{18}$ cm^{-3}) we got S=130 mV/dec, V_{th}=1.9 V and g_m=70 mS/mm with n^+ polysilicon gate material.

When the channel length of a MOSFET is scaled down, the electric field at the drain-sided end of the channel will influence the source potential and lower the effective barrier for the carriers (DIBL, drain induced barrier lowering). Homojunction MOSFETs with very short channel lengths therefore usually suffer from high off-state currents. Thermal excitation of carriers across the source-channel barrier which is determined by the built-in potential at the source-channel homojunction is responsible for this behaviour. As the off-state current depends exponentially on the effective barrier height, the introduction of a vertical heterojunction MOSFET can be an attractive alternative to decrease the DIBL effect [5].

C. Vertical SiGe Hetero MOSFETs

The modification of the typical vertical MOSFET structure by adding an undoped SiGe intermediate layer yields an additional potential barrier at the heterojunction which is independent from channel length and doping and is only determined by the Ge content in the SiGe layer. Fig. 7 shows the change in the off-state characteristics after the addition of a SiGe heterojunction. The simple evaluation of the heterojunction diode shows an unsymmetric I-V characteristic due to the additional hetero-barrier and significantly reduced leakage currents. Fig. 8 shows the calculated and measured off-state currents as a function of the Ge content x in the $Si_{1-x}Ge_x$ barrier layer. For device optimization the difference in barrier seen by the carriers between off-state and on-state must be as high as possible. A trade-off in the vertical Hetero-MOSFET design, especially in the choice of an appropriate Ge content in the SiGe layer, between low off-state currents and an improved subthreshold behaviour due to a high hetero-barrier has to be found which is not too high to be efficiently modulated.

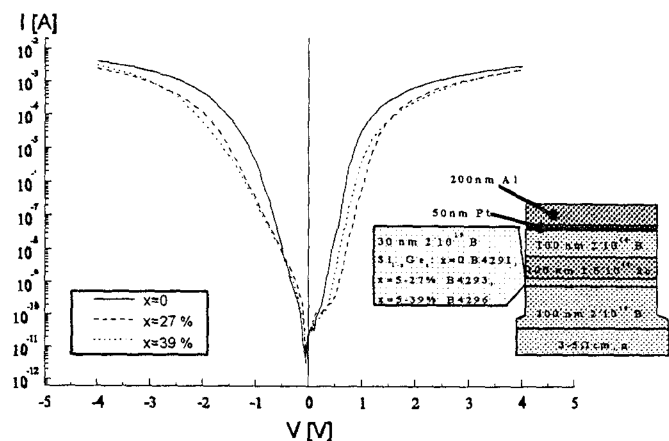

Fig. 7 Measured off-state diode characteristics of a vertical Si homojunction MOSFET in comparison with corresponding vertical Si/SiGe heterojunction MOSFET structures.

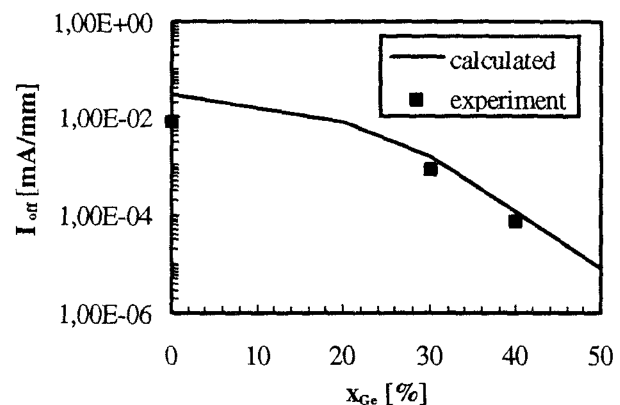

Fig. 8 Calculated off-state currents of the heterojunction diode formed in a vertical p-SiGe Hetero-MOSFET structure (channel length L=100 nm) at V_{ds}=+0.5 V as a function of the Ge content x in the $Si_{1-x}Ge_x$ hetero-barrier.

IV. CONCLUSIONS

The very good agreement of simulated and experimental data confirms the successful implementation of SiGe heterostructure physics to the available simulation tools. The promising RF performance data with calculated f_{max} values even above 100 GHz demonstrate the feasibility of these novel heterodevices for future high-speed circuits. The first 2D simulations of vertical SiGe Hetero-MOSFETs propose attractive alternatives to overcome short channel effects and scaling problems of conventional MOSFET structures and to improve the subthreshold behaviour. The used simulators have emerged as powerful tools for further device improvement.

V. ACKNOWLEDGMENTS

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