Concurrent Technology, Device, and Circuit Development for EEPROMs

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Abstract

Circuit simulation enters into a new stage of enhanced importance. From the conventional circuit simulator for circuit design an active tool for concurrent engineering is emerging, which allows to integrate technology, device and circuit development in parallel. We will show here an EEPROM development case, which has been done on a transient circuit simulation level from the beginning. A precise unified EEPROM cell model was developed describing all characteristics with surface potentials dependent on technological parameter values. This new model enabled us to realize the requested circuitry goals from the first wafer run.

1. EEPROM Characteristics

A cross-section of a generic EEPROM cell is shown in Fig. 1 [1]. The main feature of the cell is the tunneling

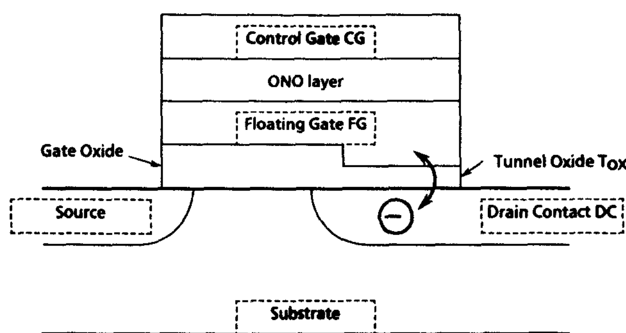

Fig. 1: Cross-section of an EEPROM cell. Charges flow from the drain contact DC through the tunneling oxide TOX into the floating gate FG and vice versa.

of charges through the oxide T_{ox} between the floating gate FG and the drain contact DC, causing a current I_{tun}. The resulting negative or positive charges on FG are responsible for a threshold voltage V_{th} shift to higher or lower values, which determines the write or erase state. To reduce the total amount of the development cost, it has been proposed to undertake concurrent engineering [2]. For this purpose a precise technology based model of the EEPROM cell is essential. Existing models mostly concentrate on a specific part of the EEPROM characteristics [3]. Our aim here is to show that a model describing the complete static and dynamic cell characteristics on the circuit level is required for the concurrent development of EEPROMs.

1.1 Technological Aspects

Fig. 2 shows the measured threshold voltage V_{th} of an EEPROM cell as a function of the charging pulse

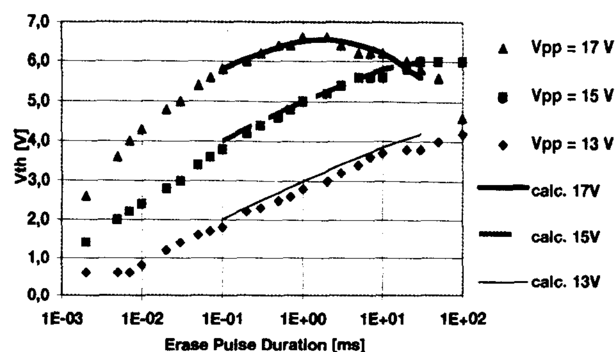

Fig. 2: Measured V_{th} curves as a function of the erase pulse duration for various pulse amplitudes V_{pp}. The symbols indicate measured points. The solid curves are simulated results.

duration for three different pulse amplitudes, 13V, 15V, and 17V. For long pulse durations with the large amplitude, a reduction of V_{th} is observed. This extraordinary transient V_{th} behavior is attributed to a transient charge loss from FG. Usually the static charge loss is measured by a 24 hours bake at 250°C, as shown in Fig. 3 [4]. From the measurement, it can be concluded that some of the FG charges are further injected into the nitride of the ONO (Oxide-Nitride-Oxide) layers during the charging operation. Due to the field applied in ONO they move further to the interface between the nitride and the top oxide. These gathered charges at the top oxide do not longer con-

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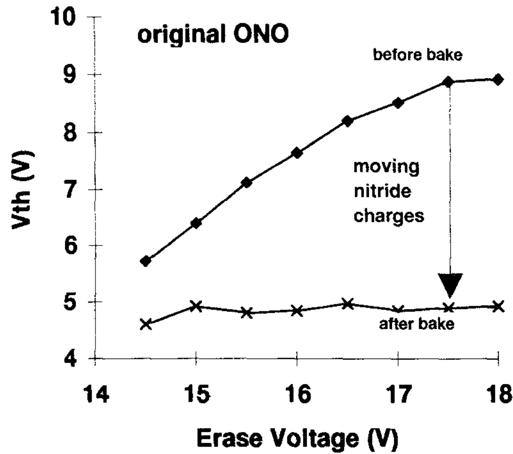

Fig. 3: Measured V_{th} curves of an EEPROM cell vs. erase voltage (1ms pulse duration) before and after a 24 hours bake at 250°C. Symbols are measured points.

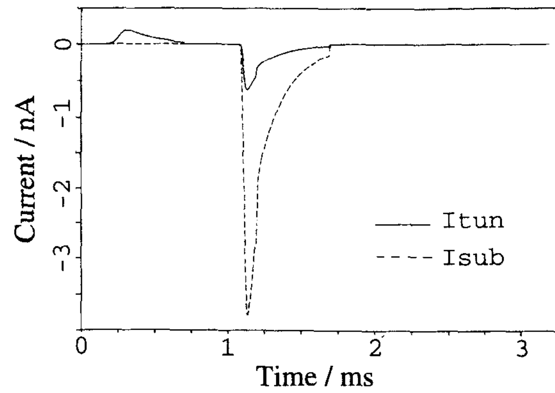

Fig. 5: Simulated transient behavior of I_{tun} and I_{sub} for an EEPROM cell at the control gate voltage of 0 and the drain voltage of 15V.

tribute effectively to a V_{th} shift. This reduction of V_{th} as a function of the pulse duration, as seen in Fig. 2, is the first direct measurement of a transient charge loss.

To prevent the charge loss from FG to ONO, the bottom oxide thickness has to be increased. Unfortunately, this measure shifts the erase/write characteristics out of its optimum, as shown in Fig. 4.

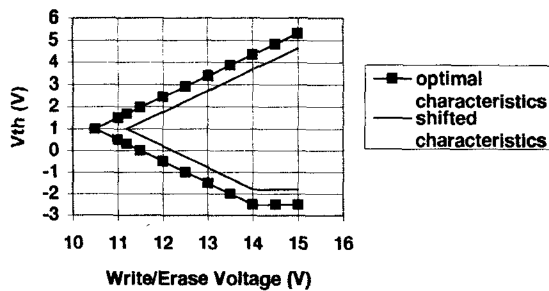

Fig. 4: V_{th} vs. erase/write pulse amplitude of an optimal EEPROM cell. The pulse duration is 1ms. By increasing the top oxide thickness in ONO the V_{th} shift occurs.

1.2 Circuitry Aspects

Fig. 5 shows the simulated tunneling current I_{tun} and the substrate current I_{sub} between DC and the substrate in the EEPROM cell. Obviously, I_{sub} can be much higher than I_{tun}. This leakage current I_{sub} must be considered in the design, where the erase/write potential is provided by on chip high voltage generators. Due to their limited strength the current flow during an erase or write cycle can saturate, especially when many EEPROM cells in the whole memory array are simultaneously selected. In Fig. 6 a simulated memory cell in a current saturation mode is shown. As can be seen, the increase of the FG potential at the beginning of an erase cycle is suppressed due to the I_{sub} contribution (indicated by an arrow), resulting in a poor erasing performance. Optimization of the doping concentration under the tunneling oxide T_{ox} is undertaken for an improvement.

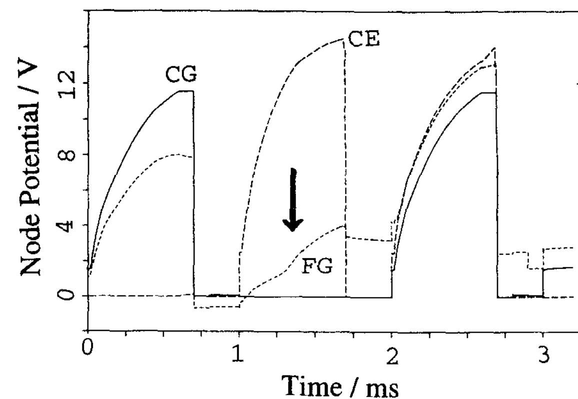

Fig. 6: Simulated transient behavior of a memory cell (EEPROM cell inclusive select transistor). CG, FG, and CE are the voltages of the control gate, floating gate, and column electrode, respectively.

2. A Model for the EEPROM Cell

Concurrent engineering in EEPROM development requires an extended circuit model to treat all features of the EEPROM cell. The developed circuit diagram is shown in Fig. 7. In addition to conventional EEPROM equivalent circuits, the charge injection from the FG node into ONO and the movement of these charges in the nitride are explicitly introduced. For the intrinsic MOS transistor part a MOSFET model based on the drift-diffusion approximation is included [5]. This model describes all device characteristics by surface potentials in the channel, which are computed iteratively during simulation. These surface potentials are a function of technological parameter values. Therefore, the parameter values of the model coincide with the measured technological data directly. This is an important aspect for a successful concurrent engineering, that attempts to optimize the technological parameter values for meeting prescribed circuit specifications.

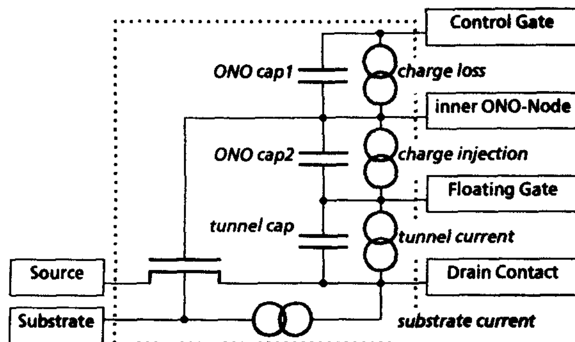

Fig. 7: Our equivalent circuit of the EEPROM cell, as used for these investigations. In addition to a conventional EEPROM model, the charge movement in ONO is included. The charges moved towards the control gate, which do not longer contribute to the V_{th} shift, are treated as lost into the control gate.

The current I_{tun} between FG and the drain contact DC is modeled by a Fowler-Nordheim tunneling [6]. For the correct calculation of I_{tun} the surface potential of the drain contact region under T_{ox} additionally has to be computed iteratively. The ONO charges are assumed to be injected from FG through the bottom oxide into the nitride also by Fowler-Nordheim tunneling. The subsequent charge movement within the nitride is modeled by a Poole-Frenkel mechanism [7]. These charges are assumed to give no more influence on V_{th}. The leakage current I_{sub} is modeled with a electron-hole generation mechanism caused by tunneling electrons from FG to DC.

All model equations together with the equations for intrinsic capacitances have to be evaluated simultaneously. It turned out that the usual neglection of the substrate capacitance C_{Fsub} between FG and substrate results in inaccurate results for I_{tun}. Therefore, the optimization has to be done not only locally between FG and DC but for the complete EEPROM cell.

For successful parameter extraction a new methodology had to be developed, which includes the design of special test structures. The extraction has to be composed of two stages, one on a static level and one and a transient level. The intrinsic transistor part can be fitted on a static level. For this purpose standard MOSFET test structures with a directly accessible gate node are required. In the next step, the Fowler-Nordheim tunneling parameters between FG and DC are extracted from a test structure, again with a directly accessible gate contact. The extraction of model parameters for the charge injection into the nitride in ONO and for their further movement in the nitride to the top oxide has to be performed with the whole EEPROM cell. This can be done only on a transient level with a circuit simulator, since the charge movement causes a simultaneous field change, which conversely is responsible for the injection characteristics. The parameters are fitted to the measured transient V_{th} behavior shown in Fig. 2.

3. Optimization Result

A static device simulation alone did not provide sufficient hints, which process modifications would be most advantageous for overall optimization of the EEPROM cell. However, transient circuit simulations with our model described above suggested that a reduction of T_{ox} from 8.5nm to 8nm would compensate nicely the shift of the characteristics due to the ONO modification. Fig. 8 depicts the charge retention results after the optimization, which is the expected goal, namely no significant charge loss with pulse amplitudes below 15V. At the same time the reduction of I_{sub} strengthened the EEPROM circuit performance without necessity to increase the driving capability of the voltage generators. The optimized result is shown in Fig. 9.

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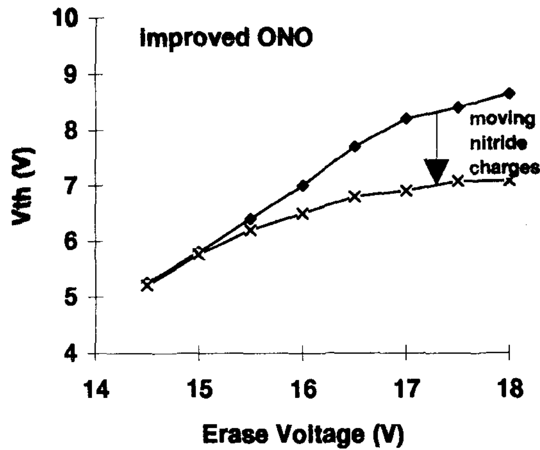

Fig. 8: Measured V_{th} curves of an optimized cell under the same condition as in Fig. 3. Here, the V_{th} shift by baking is observed only at very high erase pulses > $15V$, which are beyond standard operating conditions.

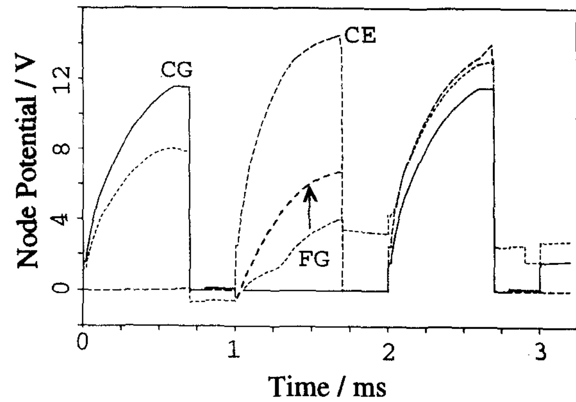

Fig. 9: Improved EEPROM cell characteristics.

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