A Pocket Implant Model for sub 0.18 micron CMOS Process Flows

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Abstract--In this paper we present a method of arriving at dopant distributions required for accurate performance estimation of 0.18 micron CMOS flows with pocket implants. Dopant profiles are calculated using a combination of physical and phenomenological models and measured device performance data. The method is demonstrated for NMOS and PMOS devices with varying pocket implant doses, energies and angles; and scaled supply voltages.

INTRODUCTION

Pocket implants are being considered in CMOS process flows designed to meet device requirements at the 0.18 micron technology node and beyond. The dose, energy and angle of the pocket implants are varied to achieve suitable two dimensional (2D) dopant distribution to meet device performance criteria. In order to understand the process to profile dependence, several techniques are being developed to determine the 2D doping profiles in these small dimension devices. These include both direct profile measurement techniques and physically based process simulators. In this paper we present a pocket implant model that can be used to arrive at 2D dopant profiles required for device simulation.

We use a combination of physical and phenomenological models to arrive at the 2D dopant profiles required for device simulation. The procedure used to arrive at the 2D dopant profile consists of two steps. First, the as-implanted 2D profile is determined using a physically based simulator. Second, the as-implanted profile is corrected for the effects of thermal cycles by using a combination of physical and phenomenological models. This approach does not use any 2D process simulation tools, has few parameters and can be calibrated rapidly.

MODEL FOR POCKET IMPLANTS

In the 0.18 micron CMOS process presented, boron pocket implants are used for NMOS devices and phosphorus implants are used for PMOS devices [1]. The as-implanted 2D boron pocket profile is estimated using the UT MARLOWE monte carlo ion implantation package [2, 3]. Fig. 1 shows the structure used in implantation simulations for the boron pocket. Fig. 2 shows the lateral decay of the as-implanted boron profile peak as a function of distance into the mask edge for boron implants of energy E1 and E2 keV (E2 > E1). From the decay shown in Fig. 2, a lateral decay slope (modeled as a Gaussian decay) can be extracted for both implants and is shown in Table 1. As expected, the higher energy implant has a larger decay slope. This lateral slope along with the 1D profile in the non masked region is now used to describe the entire as-implanted 2D profile under the mask edge.

The effects of subsequent thermal steps on the as-implanted pocket profile is modeled by breaking the problem down into two parts. First, the 1D annealed profiles are obtained by direct metrology (SIMS) or through tuned 1D process simulators [4]. Second, the 1D profiles are modified to account for the lateral diffusion of the source/drain and pocket profiles and transient enhanced diffusion to complete the 2D profile. The interaction between the channel boron profile and S/D processing causing the reverse short channel effect in NMOS devices is modeled based on work reported in [5].

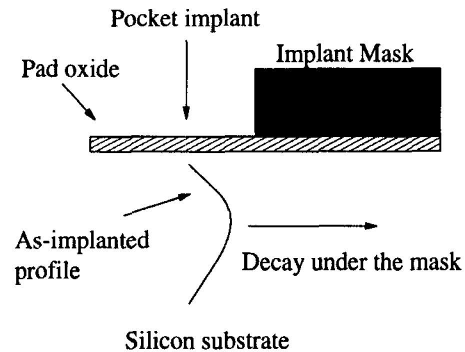

Fig. 1. Structure used for boron pocket ion implantation simulation.

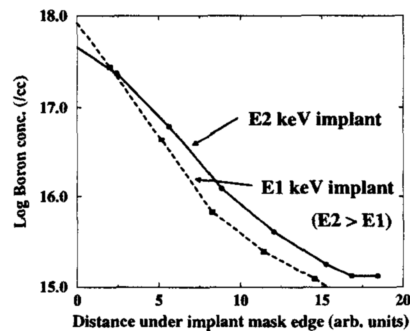

Fig. 2. Lateral decay of boron pocket implant peak under implant mask.

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Table 1. Lateral decay slopes for boron pocket implants.

Boron implant energy (keV)	As-imp. slope (arb. units)	Final slope (arb. units)
E1	0.058	0.066
E2	0.070	0.084

(E2 > E1)
Pocket 1: Low dose @ E2 keV.
Pocket 2: High dose @ E2 keV.
Pocket 3: High dose @ E1 keV.

NMOS DEVICE RESULTS

Fig. 3 shows the measured saturated threshold voltage (Vtsat) and linear threshold voltage (Vtlin) versus gate length for high and low Vt dose devices (Vd = 1.5 V) with E2 keV pocket implant. The value of the lateral decay parameter for the pocket implant is extracted from device simulations for the high Vt dose device. This value is then used in predicting the performance of the low Vt dose device and the model predictions are shown in Fig. 3. The very same extracted values are used in modeling another set of high and low Vt dose devices with a E2 keV pocket implant but of higher dose and the comparisons are shown in Fig. 4. In Fig. 5 the lateral decay parameter is extracted from the high Vt dose device

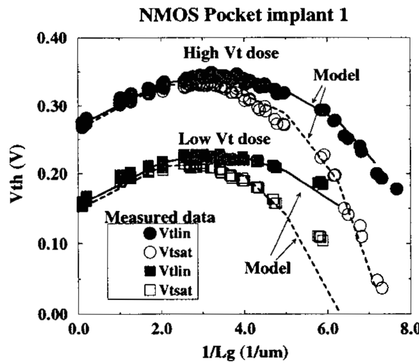

Fig.3. Threshold voltage as a function of gate length for high and low Vt dose NMOS devices with pocket implant 1.

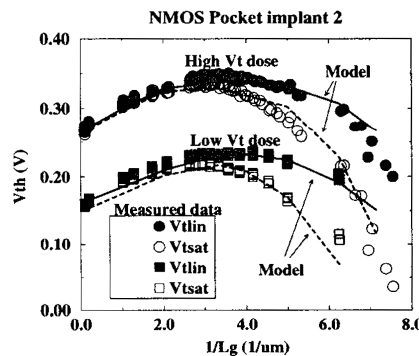

Fig. 4. Threshold voltage as a function of gate length for high and low Vt dose NMOS devices with pocket implant 2.

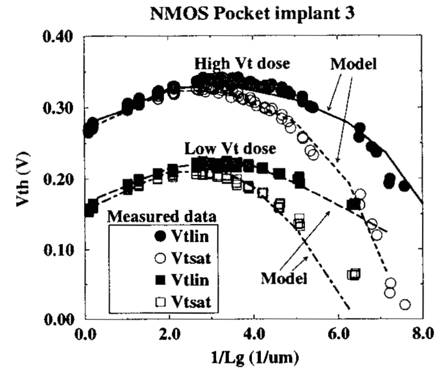

Fig. 5. Threshold voltage as a function of gate length for high and low Vt dose NMOS devices with pocket implant 3.

with a E1 keV pocket implant and is used in predicting the performance of a low Vt dose device. Fig's 3, 4 and 5 show that the extraction procedure used can model device data for gate lengths between 0.14 micron and 5 microns. This demonstrates that the model can be extended to sub 0.18 micron CMOS process flows. Fig. 6 shows a comparison between measured and modeled Vtsat and (Vtlin - Vtsat) a measure of drain induced barrier lowering (DIBL) for devices discussed in Fig. 3. Fig. 7 shows the off current (Ioff) and Fig. 8 the drive current (Ion) as a function of gate length for the devices shown in Fig. 3.

The good match between the model predictions and measured data indicates the validity of the method and the final values of the lateral decay parameter used in device simulation. Using the information from Table 1, the performance at other pocket implant energies can be predicted as follows: calculate the as-implanted lateral decay slope using the ion implantation simulation, and model the effects of thermal annealing using the empirical relationship shown in Table 1.

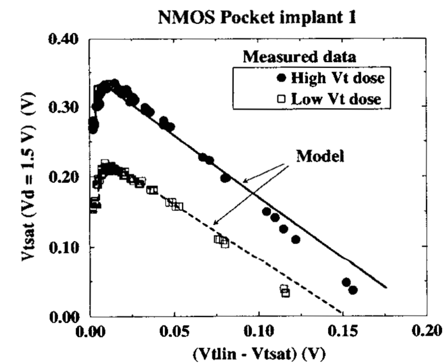

Fig. 6. Vsat vs. (Vtlin-Vtsat) for NMOS devices with pocket implant 1. (Vtlin-Vtsat) is a measure of DIBL.

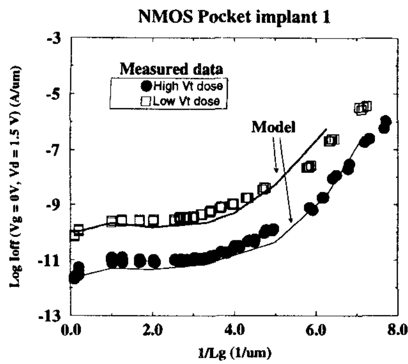

Fig. 7. Off current (Ioff) Vs. Gate length for NMOS devices with pocket implant 1.

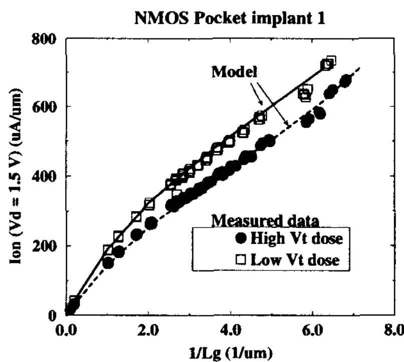

Fig. 8. Drive current (Ion) vs. Gate length for NMOS devices with pocket implant 1.

PMOS DEVICE RESULTS

The same procedure is applied to PMOS devices with an angled phosphorus pocket implant 4. The results are shown for devices designed for both 1.0 and 1.5 V operation. Pocket parameters extracted from the 1.0 V device are used in predicting the performance of the 1.5 V device. Figs 9, 10 and 11 show the comparison between measured and modeled parameters for both the 1.0 and 1.5 V device. These results demonstrate that the method can be extended to devices designed for different supply voltages.

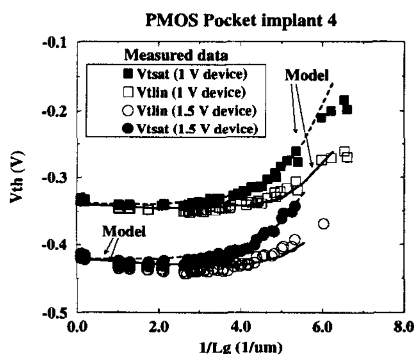

Fig. 9. Threshold voltage as a function of gate length for 1.0 and 1.5 V PMOS devices with pocket implant 4.

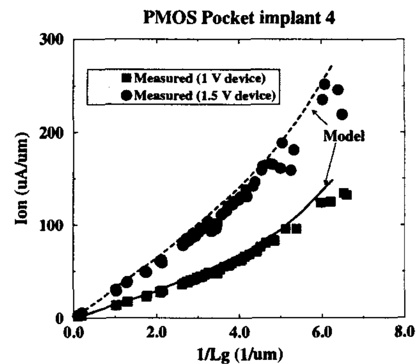

Fig. 10. Drive current (Ion) vs. Gate length for 1.0 and 1.5 V PMOS devices with pocket implant 4.

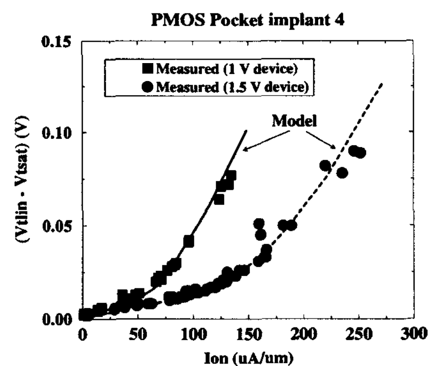

Fig. 11. (Vtlin-Vtsat) vs. Drive current (Ion) for 1.0 and 1.5 V PMOS devices with pocket implant 4.

CONCLUSION

A method to arrive at 2D dopant profiles for sub 0.18 micron CMOS process flows with pocket implants is presented. The method is demonstrated for NMOS and PMOS devices with different pocket implant conditions and scaled supply voltages.

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