Extended Anisotropic Mobility Model Applied to 4H/6H-SiC Devices

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Abstract—We present an extended mobility model that accounts for anisotropic current transport along non-equivalent crystallographic axes for a given wafer orientation. Using this model we investigated the influence of anisotropic effects on the device characteristics of 4H- and 6H-SiC transistor structures (JFET, UMOS, DIMOS). Dependent on the polytype of the underlying material and the device structure, large variations in the device behavior may result from anisotropic mobility. This influence is strongest in the 6H-SiC DIMOS.

I. Introduction

For special electronic applications in the high-power, high-temperature or high-frequency regime, semiconductor devices based on wide-bandgap materials such as silicon carbide (SiC) offer promising properties. In the past decade, a large variety of devices were proposed to exploit the attractive features of SiC [1] which include a high thermal conductivity ($4.9\,W/cm\,K$), saturation velocity ($2.7 \cdot 10^7\,cm/s$) and electric breakdown field ($2-3\,MV/cm$). The numerical simulation of such wide-bandgap devices requires the availability of advanced physical models, which are flexible enough to describe the pecularities of certain material properties as, e.g., the anisotropic mobility of carriers.

A flexible mobility model allowing for anisotropic current transport along non-equivalent crystallographic axes for a given wafer orientation has been implemented in the multi-dimensional device simulator DESSIS$_{-ISE}$ [2]. The model is able to describe the anisotropic current transport for a given material by specifying different mobility tensor elements along the respective crystal directions.

With the hexagonal polytype as basic material, the effect of anisotropy observed in different device structures varies with the ratio of vertical to lateral current flow as well as with the orientation-dependence of the basic physical parameters. The performance of devices such as pn-diodes and Schottky-diodes, which exhibit a predominantly one-dimensional current flow, can be easily optimized by choosing the appropriate crystal direction for the current flow. But considering the effect of anisotropic mobility on more complex device structures, it turns out that a very careful analysis of the device operation is needed for an optimum design. Large progress has been made in fabricating such devices [3], which among others, exhibit a significantly reduced on-resistance compared to state-of-the-art silicon devices [4]. Our study demonstrates that, depending on the polytype of the underlying material and the device structure considered, large variations in the device performance may result from anisotropic mobility.

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II. Modeling

Within the framework of phenomenological transport theory [5], the isothermal drift-diffusion current relations for electrons and holes have to be extended to tensor equations

$$\vec{J}_\alpha = q\, c_\alpha\, \tilde{\mu}_\alpha\, \vec{\nabla}\phi_\alpha,\ (\alpha = n,\, p) \tag{1}$$

where $\tilde{\mu}_\alpha$ denotes the mobility tensor, c_α the density and ϕ_α the quasi-Fermi potential for electrons and holes, respectively, while q is the elementary charge.

We use the same discretization scheme as in the case of galvanomagnetic current transport [6]. Since, in general, the wafer orientation and the device coordinate system does not coincide with the crystallographic axes of the semiconductor lattice, an orthogonal transformation $\tilde{D}$ has to be employed

$$\tilde{\mu}^0_\alpha = \tilde{D}\, \tilde{\mu}_\alpha\, \tilde{D}^t \tag{2}$$

to obtain the anisotropic mobility tensor in diagonal form. Here, $\tilde{D}$ describes the three-dimensional rotation transforming the device coordinate system to the crystal axes. For the hexagonal modifications of SiC, $\tilde{\mu}^0_\alpha$ has only two independent diagonal elements

$$\tilde{\mu}^0_\alpha = \begin{pmatrix} \mu_\perp & 0 & 0 \\ 0 & \mu_\perp & 0 \\ 0 & 0 & \mu_\parallel \end{pmatrix} \tag{3}$$

with $\mu_\parallel$ parallel and $\mu_\perp$ perpendicular to the ĉ-axes, respectively [7]. This is a simple consequence of crystal symmetry. Applying (2) then gives all coefficients of the mobility tensor $\tilde{\mu}_\alpha$ in the device coordinate system.

The anisotropy of mobility results from the anisotropic electronic structure in non-cubic crystals which, among others, leads to different effective masses and scattering rates along inequivalent high-symmetric directions. Up to know, microscopic semiconductor transport theories do not give a quantitative description of the anisotropy in SiC. On the other hand, numerous measurements have been reported for the mostly used hexagonal polytypes

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4H- and 6H-SiC, finding a ratio of $\mu_\perp/\mu_\parallel = 5$ for 6H-SiC and $\mu_\perp/\mu_\parallel = 0.8$ for 4H-SiC [8], [9].

The implemented model accounts for the dependence of mobility on doping concentration and high electric fields [2]. As Monte Carlo simulations indicate [10], the saturation velocities perpendicular and parallel to the ĉ-axes have slightly different values, which had to be properly included in the high-field mobility model.

III. Simulation and Results

In the recent years, several promising device structures have been realized to explore the potential of SiC power devices. Examples include the junction field effect transistor (JFET), the trench-gated MOS (UMOS) and the double implanted MOS (DIMOS) transistor [3]. The schematic of these device structures is shown in Fig.1.

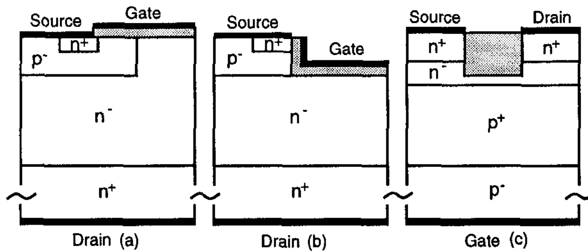

Fig. 1. *Schematic of the simulated DIMOS (a), UMOS (b) and JFET (c) structures.*

All of them are equiped with a substrate contact which enables vertical current flow or potential control and, therefore, allows reduced cell sizes. The JFET (c) uses the substrate contact as gate electrode controlling the current in lateral direction. The UMOS, on the other hand, is controlled by a vertical gate electrode (b) whereas the DIMOS is controlled by a lateral gate electrode (a), with the drain contact on the substrate.

The wafer surface of industrial fabricated substrates is usually oriented perpendicular to the ĉ-axes of the crystal. Therefore for all simulations $\mu_\perp$ is assumed to be the mobility parallel to the wafer surface. From measured doping dependent bulk electron mobilities we extract a ratio of $\mu_{4H,\perp}/\mu_{6H,\perp} = 2.3$. This is the factor by which we have to scale down the results of the 4H-SiC simulations in order to get a proper comparison with the I-V-characteristics of the 6H-polytype. In addition, we assume anisotropic saturation velocities.

The resulting output characteristics of the JFET for two gate voltages are shown in Fig. 2. The anisotropy of the 6H-SiC polytype leads to a higher resistance of the n^- epi-layer underneath the n^+ contact implantation layers and therefore to a slight decrease of drain current. But it is the degradation of the effective channel mobility caused by the $SiC - SiO_2$ interface which dominates the current transport characteristics.

Different to the JFET, the current flow in the UMOS (Fig.3) is mostly oriented in vertical direction. The 4H-SiC structure is superior to the 6H-polytype in consequence of the higher vertical mobility $\mu_\parallel$. This finding is corroborated by comparing the simulation for 6H-SiC

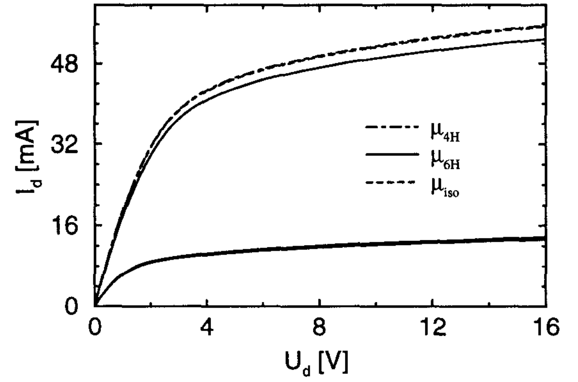

Fig. 2. *Output characteristics of the JFET for $U_G = 0\,V$ (upper curves) and $U_G = -2\,V$ (lower curves).*

with an isotropic calculation using a reduced mobility of $\mu = 0.2\,\mu_\perp$, which is shown to be a quite good approximation. The resulting specific on-resistance will be slightly overestimated because of the lateral components of current flow in the drift zone beneath the trench.

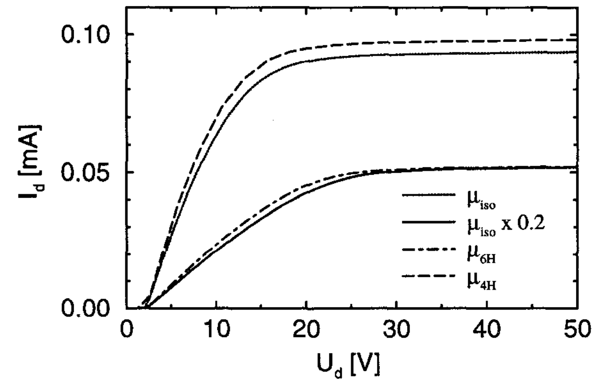

Fig. 3. *Influence of anisotropic mobility on the UMOS output characteristics at $U_G = 20\,V$.*

Finally, in the DIMOS, the current flows partly in lateral, partly in vertical direction. The saturation current is determined by the saturation velocity and the resulting field-dependent effective channel mobility $\mu_\perp$. Neglecting the influence of contact resistances and the bulk resistance of the substrate, the on-resistance of the device originates from mainly three parts [11]: The resistance R_E of the enhancement-mode FET between source and the pn-junction underneath the gate, the JFET resistance R_{jfet} of the region near the pn-junction, and the bulk resistance R_{epi} of the n^- drift zone (Fig.1). As a result of the predominantly vertical current flow in the JFET region and drift region, the reduced vertical mobility of the 6H-polytype significantly increases R_{jfet} and R_{epi}, thus leading to a higher on-resistance of the entire device (Fig.4). In this case, an isotropic simulation with $\mu = 0.2\,\mu_\perp$ clearly demonstrates that this structure cannot be properly analysed without inclusion of orientation-dependent mobility.

This is confirmed by comparing the flowlines obtained from an isotropic mobility $\mu_0 = \mu_\perp$ with those resulting from the 6H-SiC anisotropy (Fig.5). Because of the larger

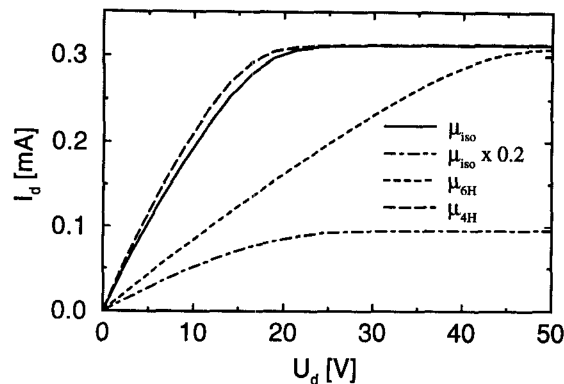

Fig. 4. *Influence of the anisotropic mobility on the DIMOS output characteristics at $U_G = 20\,V$.*

mobility in lateral direction parallel to the surface, the current flow is distributed by an angle up to 15 degree in the drift region.

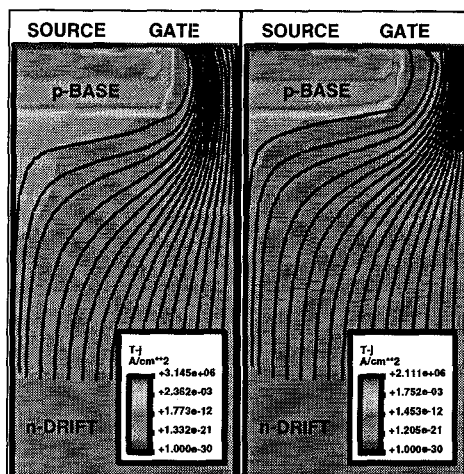

Fig. 5. *Current flow lines of the lateral VDMOS excluding (left) and including (right) anisotropic mobility.*

Consistent with the above results, the higher vertical mobility of the 4H-polytype leads to a reduced on-resistance of the device (Fig.4).

The major advantage of the DIMOS is that this device does not suffer from decreased channel mobilities, as it is the case along the vertical MOS interfaces formed on the sidewalls of the trench of the UMOS. Besides it is also avoided that the breakdown voltage is reduced by high-field stressing of the oxide at the corners of the UMOS trench. Recently the first realization of such a device has been published [12]. The simulated specific on-resistance of the two-micron channel length DIMOS is in good agreement with the reported value of $66\,m\Omega/cm^2$. The anisotropic characteristic of the 6H-SiC used for this device reduces the on-resistance by about 34%. A reduced effective channel mobility caused by the $SiC - SiO_2$ interface increases the influence of R_E with respect to the other contributions to the entire on-resistance. Hence, should the effective channel mobility be improved by further technological progress, the effect of anisotropy will be even more significant.

IV. Conclusion

We demonstrated the relevance of anisotropic mobility modeling with reference to different representative 4H- and 6H-SiC devices. It shows that in consequence of its higher mobilities, the static behavior of vertical 4H-SiC devices is in general superior to the respective 6H-polytypes. In addition, the anisotropic mobility may significantly deteriorate the device performance. This disadvantage of 6H-devices can be weakened by the use of structures with predominant lateral current flow such as the JFET.

Our studies also show that an accurate analysis of devices with anisotropic transport properties cannot be obtained by rescaling the isotropic mobility models. Instead, a full tensorial formulation of the constitutive current relation has to be employed. The implemented model can easily be extended to other non-cubic materials.

Acknowledgment

The authors are grateful to N. Kaminski, A. Schenk, K. Gärtner, U. Krumbein for providing helpful advice and the ISE for providing software facilities.

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