

A Computationally Stable Quasi-Empirical Compact Model for the Simulation of MOS Breakdown in ESD-Protection Circuit Design

Shiang Liang Lim*, Xin Yi Zhang, Zhiping Yu, Stephen Beebe*, and Robert W. Dutton

*Now with Tritech Microelectronics, Singapore

Center for Integrated Systems, Stanford University, Stanford, CA 94305

*Advanced Micro Devices Inc. Sunnyvale, CA 943088-3453

Abstract -- This paper presents a simple-to-implement, semi-empirical model for circuit-level simulation of the MOS breakdown region, with application in ESD-protection circuit design. A new formulation for the multiplicative factor M , used to model avalanche current generation, shows good convergence properties when used in circuit simulators. The effects of source/drain series resistance, substrate resistance, and the parameters of the new M expression are described. We describe how to calibrate the parameters for a NMOS device. Finally, we compare the simulated results with experimental data.

I. INTRODUCTION

Modeling a transistor's I-V characteristics in the breakdown region is important for the design of electrostatic discharge (ESD) protection circuits. During an ESD stress, current and voltage levels far exceed the regions of normal transistor operation. The ability to model such high-current behavior in circuit simulators enhances fast and effective design of such protection circuits.

The MOS breakdown region can be modeled with a parasitic bipolar transistor in parallel with the MOS device, together with a current-controlled current source that models the avalanche multiplicative effect [1]. Avalanche occurs near the drain region because of the high electric field, which causes electron-hole pair generation. The electrons flow into the drain while the holes flow through the substrate contacts.

The substrate current creates a potential drop across the substrate-source junction, and eventually turning on the parasitic NPN bipolar transistor (BJT) formed by the drain-substrate-source junctions. This in turn conducts more current and creates more avalanche-generated carriers. The positive feedback process causes the total drain current to increase sharply above the drain breakdown voltage.

Fig. 1 shows a standard circuit used to model this breakdown. The avalanche-generated current is modeled as [1]:

$$I_{gen} = (M - 1) \cdot (I_{ds} + I_c) \quad (1)$$

where I_{ds} is the MOS surface drain current, and I_c is the parasitic bipolar (BJT) collector current. The multiplication factor, M , is often written in the following form [2]:

$$M = \frac{1}{1 - K_1 \exp\left[-\frac{K_2}{V_d - V_{dsat}}\right]} \quad (2)$$

where k_1, k_2 are fitting parameters related to the drain depletion width and impact ionization coefficients, and V_{dsat} is the MOS saturation voltage. At low V_d , M is 1 or close to 1; it increases as V_d increases.

A drawback for the above expression for M is that it causes convergence problems when implemented directly in a circuit simulator such as SPICE. As V_d increases, the denominator goes to zero, thereby creating a discontinuity in M as it goes to infinity. If the initial I_{ds} and I_c are very small, as is the case when V_g is close to 0V, the parasitic bipolar will fail to turn on because the iterations may "jump" across the discontinuity. This causes SPICE to either simulate the wrong behavior or fail to converge. We observe similar problems even when V_g is more than 0.1V if the drain current step increment for the simulation is too large.

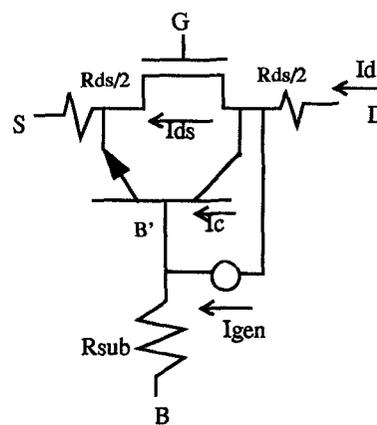


Fig. 1 Circuit schematic for simulating MOS breakdown.

Improving the convergence properties of the breakdown model would increase its usefulness and range of application. In the next section, we introduce an alternative M formulation that is more robust and simple to implement. We then describe the effects of each parameter in this new M expression, of the source/drain series resistance, and of the substrate resistance on the breakdown I-V characteristics. Next, a qualitative description of how to obtain the required parameters from experimental data is given. Finally, the simulated results are compared with measurement.

II. ALTERNATIVE M FORMULATION

The discontinuity in M can be overcome by using a continuous function:

$$M = \exp[k_1(V_d - V_{dsat} - d_1)] + \exp[k_2(V_d - V_{dsat} - d_2)] \quad (3)$$

where k_1 , d_1 , k_2 , d_2 , are parameters used to fit measurements. Two exponentials are used to approximate the M function from (2) in the region of interest, namely from $M=1$ to the point where snapback occurs. The first exponential should have a slower rate of increase relative to the second one ($0 < k_1 < k_2$), but "activated" earlier ($0 < d_1 < d_2$). The result is a reasonably smooth I-V transition from the saturation region to the start of avalanche and snapback. This formulation shows better convergence properties than (2) because of its continuity, and produces the correct I-V behavior even at $V_g=0V$, without any modification to the SPICE code. This makes it simple to implement and more robust. Like (2), it incorporates the effects of normal field dependence and saturation velocity through V_{dsat} , which to first order is given by [3]:

$$V_{dsat} = \frac{V_g - V_t}{1 + \frac{(V_g - V_t)}{L \cdot E_{sat}}} \quad (4)$$

where L is the channel length, V_t is the device threshold voltage, and E_{sat} is the saturation electric field.

III. ANALYSIS OF PARAMETERS

The k_1 and k_2 in (3) determine the rate of increase of M while d_1 and d_2 are translation factors which determine when avalanche multiplication starts to take place. Fig. 2 shows a comparison between the M factor from (2) and (3). The discontinuity in the old M occurs around $V_{ds}=9V$, which is the trigger voltage. The new M matches the old one at the trigger voltage and the holding voltage ($V_{ds}=5.5V$), thus ensuring similar trigger and holding points in the IV snapback curves. We can clearly see the two regions where each of the exponential functions is dominant.

As shown in Fig. 3, K_2 affects the "width" of the snapback region, i.e. $V_{trigger} - V_{hold}$, for $V_g=0V$. This can be explained by first noting that since the total generated current is very small, a sufficiently high M is needed to generate enough substrate current to forward-bias the parasitic BJT [1]. Our simulations show that this occurs for $V_b \sim 0.8V$. Since M increases more slowly for a smaller k_2 , a higher V_d is needed to achieve the required M .

Since d_2 determines when the avalanche multiplication starts generating electron-hole pairs significantly, we expect

it to shift the snapback trigger point correspondingly as shown in Fig. 4.

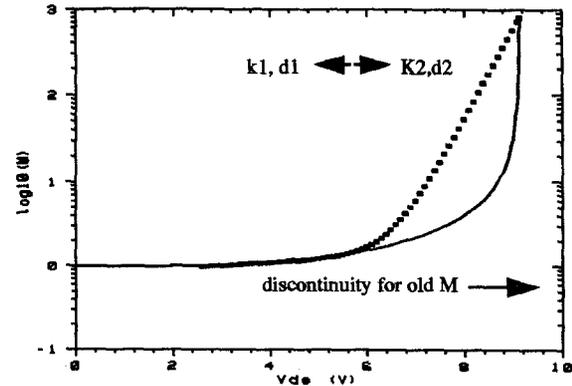


Fig. 2 Comparison between old, discontinuous M (line) and new, continuous M (squares). The point of discontinuity and the region where the new M parameters are dominant, are indicated.

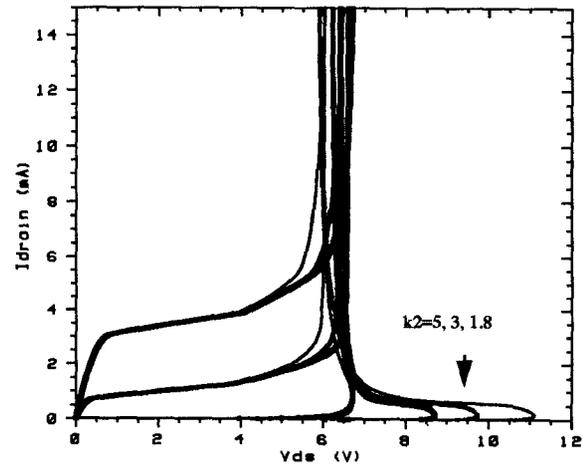


Fig. 3 Variation of snapback width with k_2 . A lower K_2 leads to a wider snapback curve. The gate voltage is stepped from $0V$ to $1.5V$ in increments of $0.5V$.

Note that for each set of M parameters, at all V_g 's, the current level increases rapidly around the same V_d , corresponding to values of M that agree well with a second condition for current regeneration using positive feedback analysis [1]:

$$M = \frac{1}{\beta} \quad (5)$$

where β is the current gain of the parasitic BJT. This corresponds to the case when the current feedback loop gain is $+1$; hence, the current will increase indefinitely. K_1 and d_1 affect

the M factor between 1 and the point where the current increases dramatically, as given by (5). In other words, $k1$ and $d1$ should only matter at the onset of avalanche, by affecting where and how fast the output conductance starts increasing as shown in Figs. 5 and 6.

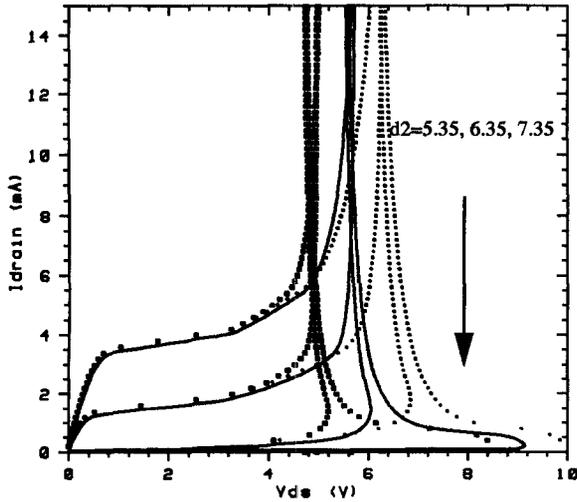


Fig. 4 Variation of snapback trigger voltage with $d2$. Larger $d2$ increases snapback trigger voltage.

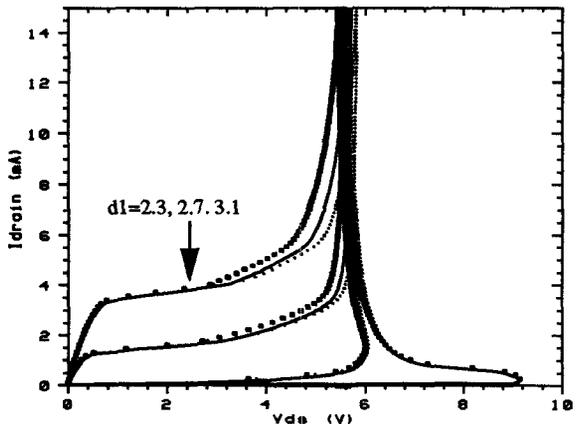


Fig. 5 Effect of $d1$ on the onset of avalanche. Increasing $d1$ delays the start of avalanche.

In addition to the M parameters, correctly modeling key resistance such as the substrate resistance (R_{sub}) is also important, especially in high current regimes. R_{sub} is the bias resistance for the emitter-base junction of the parasitic BJT. The drain and source resistances (R_{ds}). At high current levels, the extrinsic resistance dominates the intrinsic device resistance and hence determines the I-V slope. To provide

more uniform turn on of multi-finger ESD protection structures, increasing R_{ds} is used as a technique for increasing the ballast resistance of the fingers.

Fig. 7 shows that a larger R_{sub} decreases the “height” of snapback. To turn on the bipolar device at a lower R_{sub} , a higher trigger currents needed to forward bias the parasitic base-emitter junction. Hence, R_{sub} can be used as an additional parameter in modeling the snapback region.

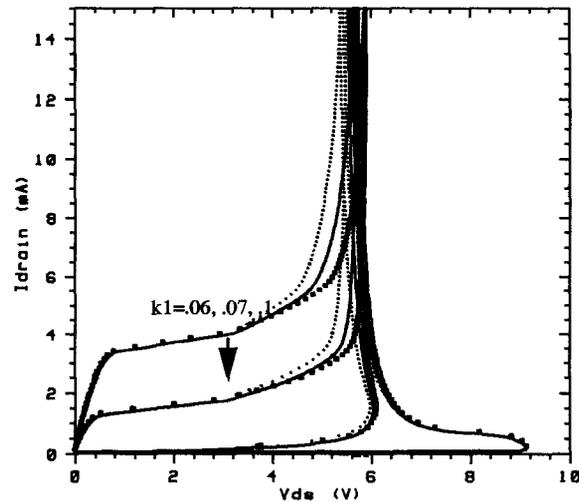


Fig. 6 Effects of $k1$ on the onset of avalanche. Increasing $k1$ increases output conductance at the onset of avalanche.

III. CALIBRATION AND RESULTS

Comparison of simulated results using the original M in (2) and the new M formulation in (3) is shown in Fig. 9. The lowest V_g used was 0.12V since (2) does not produce correct behavior for $V_g < 0.1V$. For $V_g = 0.12V$, the snapback curve from (2) is higher than that from (3) because the original M (2) is less than the new expression M (3). Hence, for a given drain current, a higher V_d is required for (2) to produce the same level of avalanche multiplication. In addition, the increase in drain current at the onset of snapback is less abrupt using (3) than (2), a result which is more consistent with measurement data.

Comparison of simulation results with measurements is shown in Figure 10. Tests were done on a $20\mu/0.35\mu$ NMOS device. There is a good match for both the triggering voltage and current at $V_g = 0V$. Also, at higher V_g the transition into the avalanche region is good. The avalanche turn-on voltage for the different V_g 's corresponds to $M \sim 1.3$. This is consistent with the use of $\beta = 3$ in our BJT model (from (4)).

The calibration process begins from the M in (2), which can be extracted using the methodology outlined in [2]. By fitting M near the holding and trigger voltage using $k2$ and $d2$ and fitting the output conductance at the beginning of the

avalanche using $d1$ and $k1$, we can obtain good fit with experiments. In addition, R_{sub} and R_{ds} can be used to further improve data matching. For our measured device, we used $d2=6.7V$, $k2=1.8V^{-1}$ and $R_{sub}=1k\Omega$ to achieve an acceptable fit in the snapback region for $V_g=0V$. For $V_d=4V$, we used $k1=0.07V^{-1}$ and $d1=3.5V$ to achieve a good fit in that region.

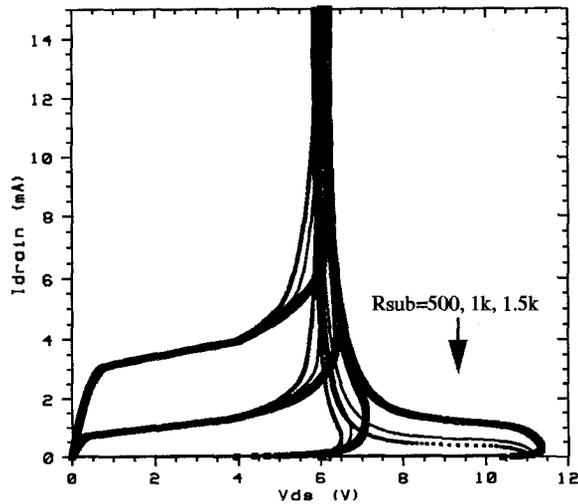


Fig. 7 Variation of snapback height with R_{sub} . Increasing R_{sub} decreases snapback height.

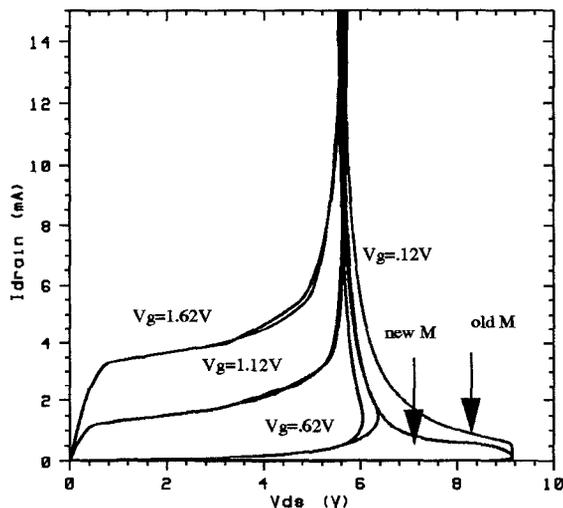


Fig. 9 Comparison of snapback curves obtained using old M (2) and new M (3).

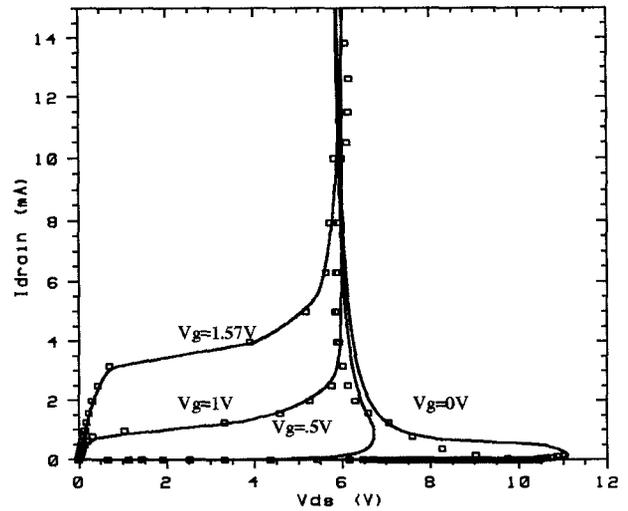


Fig. 10 Comparison of simulation (line) and measurement (square) results.

CONCLUSION

We have presented a more robust, computationally stable formulation for the avalanche multiplicative M factor used in circuit modeling of MOS breakdown. This has useful applications for the design of ESD-protection circuits. Its continuity throughout all voltage range makes it more robust for circuit simulators and improves convergence. The impact of each model parameter on the IV curve was described, and the explanation for these effects are consistent with reported research. Finally, good agreement was obtained by calibrating the model to measurement results.

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