Capacitive detection method evaluation for silicon accelerometer by physical parameter extraction from finite element simulations

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***Abstract*—A capacitance evaluation method based on the extraction of physical parameters from finite element (FE) analysis is presented. Mechanical simulations and this capacitance evaluation method were applied to a new, highly symmetrical, silicon accelerometer in view of globaly modeling the sensor system. The commercial hardware description language HDL-A^{TM} is used to develop a compact behavioral macro-models for SPICE simulators.**

I. Introduction

The modeling and simulation of microsystems follows a logical development flow:

1. layout and design (mask editing and design rule checkers)
2. process simulation (semiconductor process simulation and etch simulation)
3. device simulation (FEM, BEM field solvers and analytical methods)
4. system simulation (SPICE and HDL techniques)
5. global simulation (iteration of the above steps).

Many tools exist at these various levels of simulation. For a comprehensive overview, the reader is referred to [1]. Seamless data transfer between the levels is required to accelerate development time and extend the usefulness of simulation. Challenges include geometric construction from mask and process data, 3D coupled field simulation, construction of lumped macro models, and computer aided insertion of those macro models into dynamical simulators [2]. This paper describes a physical parameter extraction approach and associated numerical tools [3], developed to address the passage of device models from the device simulation level [4] to the system simulation level. A commercial finite element package (ANSYS^{TM}) which has become a standard in the field because of its comprehensive coupled field capabilities, is used as the field solver for device simulations. A commercial hardware description language (HDL), HDL-A^{TM} of Anacad Engineering^{TM}, is used for the system level models of microsystem devices [5]. The methodology and software tools are generic with respect to numerical field solvers and analog HDLs interfaced with SPICE simulation tools. A silicon (Si) micromachined accelerometer using capacitive detection is presented as an application example [7].

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II. Physical parameter extraction

A physical parameter extractor (**PXT**) based on the numerical integration of nodal (and element) degrees of freedom (DOF) has been developed, and interfaces with ANSYS. In the case of static FE analysis, the flow (current, force, torque, flow rate, heat flow rate, etc.) variable is calculated for a given effort (voltage, translational velocity, rotational velocity, pressure, temperature, etc.) variable. A physical macro-parameter (resistance, capacitance, reactance, displaced volume, electrostatic force etc.) can also be calculated for given boundary conditions. By iterating the variation of boundary conditions and extracting the physical quantity of interest, a piecewise-linear macro-model describing the behavior of a device is created. A behavioral HDL-A model is then generated for the SPICE simulator. Digital synchronization is used to ensure sufficient precision during simulation [6].

For a harmonic FE analysis, **PXT** may again be used to integrate spatial DOFs in order to derive macro-values. The result is a piecewise linear macro-model describing the frequency response (amplitude and phase) of the model. A polynomial fit is performed, and a behavioral HDL-A model is generated, using a polynomial filter (transfer function) approach. HDL-A models derived from both static and modal FE analyses are valid for the dc, ac and transient SPICE analysis domains, and are different representations of the behavior of a given device.

III. Capacitive accelerometer application example

A new bulk-microfabricated Si accelerometer developed at LPMO, Besançon, France is presented as an application example. The design enables very low cross-sensitivities as well as a batch fabrication processing of the whole device. The structure consisting of a seismic mass suspended by four thin beams is presented in fig. 1. The sensing axis of the sensor is contained in the wafer plane and is perpendicular to the beams. This structure was fabricated by double side etching of a <100> silicon wafer, and a non conventional alignment of (45° from the <110> wafer flat

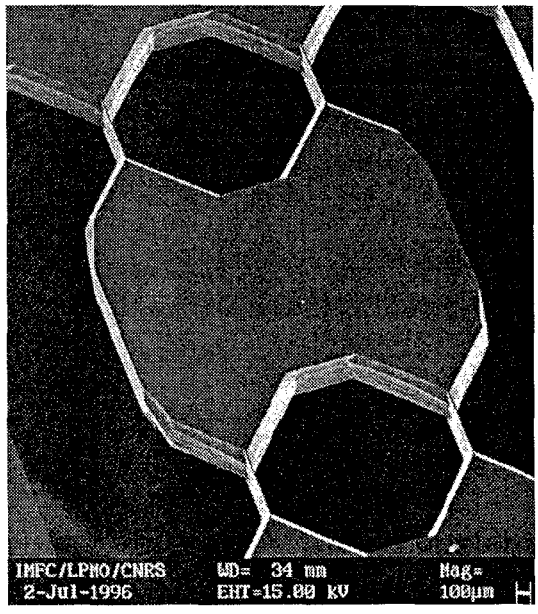

Fig. 1. SEM photograph of the accelerometer.

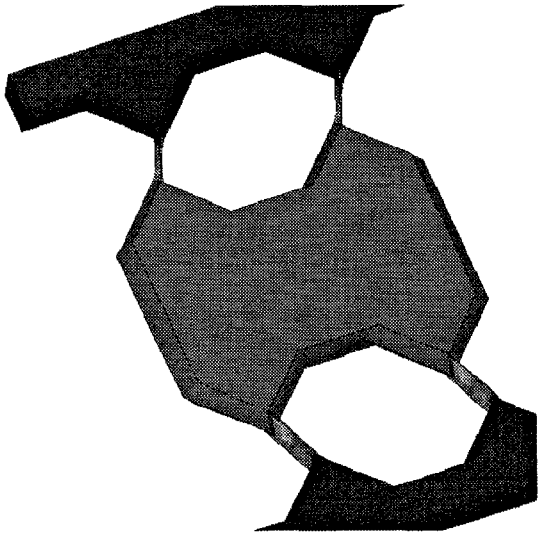

Fig. 2. FE analysis of the device under an in-plane acceleration.

to fabricate two perpendicular devices on one wafer in the same KOH-solution etching step.

Fig. 2 shows the FE model used to characterize the mechanical behavior of the device using harmonic analysis. Electrostatic field simulations were performed in ANSYS to optimize the capacitive response of the detection electrodes whose design is presented in [8]. This capacitive detection is based on measuring the capacitance change between a movable electrode and a reference electrode. The two electrodes are designed like fine-tooth comb made of several hundred segments. Figure 3 show the calculated electric field between opposite electrode segments.

The capacitance C between two ideal conductors may

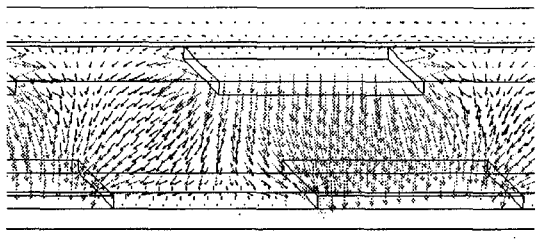

Fig. 3. Detail of 3D electrostatic FE model and simulated electric field between opposite electrodes.

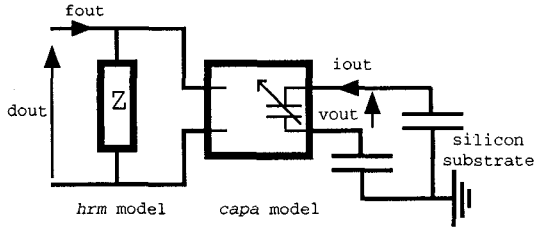

Fig. 4. Schematic of accelerometer circuit for SPICE simulator. HDL-A models are thick-rimmed boxes.

be calculated using:

$$C = \frac{\epsilon_0 \epsilon_r}{V} \int_S \vec{E} \cdot \vec{n} d\sigma \qquad (1)$$

where V is the applied electric potential, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the medium, $\vec{E}$ is the electric field, $\vec{n}$ is the surface normal and S is the surface of one of the electrodes.

The lower electrode capacitance was extracted using **PXT** (which implements a numerical integral of Eq. 1) for relative displacements of the seismic mass. A comparison with a parallel plate capacitor analytical formulae, which neglects the fringe field, has been done [8].

The simulation and capacitance extraction allowed the selection of an optimal number of electrodes and electrode width with respect to the sensitivity defined by the slope of the extracted capacitance-displacement function.

IV. HDL MODELING OF THE ACCELEROMETER

Using the mechanical data and the capacitance data, HDL-A models of the accelerometer are generated. The accelerometer device modelization has been split into two elements. Figure (4) is a schematic view of the global model accelerometer architecture. The first element is modeled as a mechanical harmonic resonator directly obtained from the structural FE simulations (fig. 5). The mathematical model used to describe the mechanical behavior of the accelerometer is a linear differential equation. From the network theory point of view, this model is a passive one-port element. The nature of the signal going through and across the pins of the one-port model are respectively the force and the displacement corresponding to the *mechanical2* nature in HDL-A.

The harmonic simulation has been done with an excitation force applied to the center of gravity of the mechanical structure of the accelerometer. The displacement

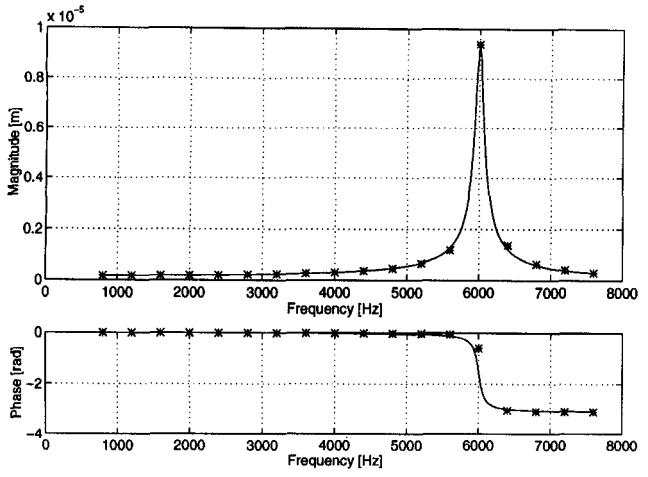

Fig. 5. FE calculated sensing axis displacement transfer function of seismic mass for an excitation force of 1.0 mN.

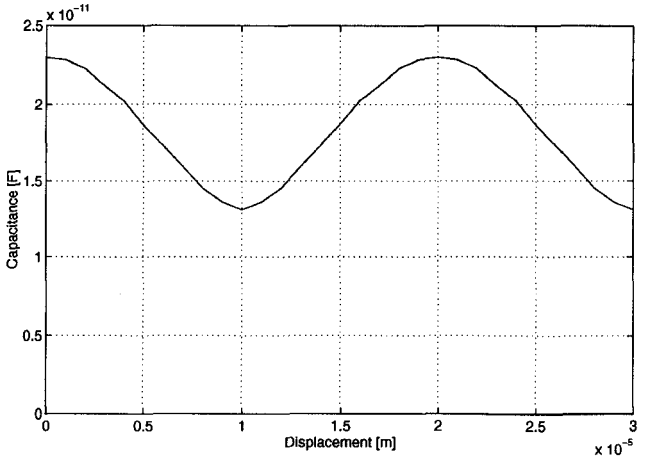

Fig. 6. Extracted capacitance as a function of displacement.

of this gravity center is picked up and transcribed into a mechanical behavioral model. The product of the applied force and the displacement is the mechanical energy received by the accelerometer. Table I is the HDL-A model listing. The parameters *coefd*() and *coefn*() and *prop* of the mechanical model are calculated automatically from FE simulation data with **PXT**. The value of the parameter F defaults to 1.0, which corresponding to an applied force of 1.0 N.

The electrical part of the model is a variable capacitor load implemented as a piecewise linear lookup table (fig. 6). The nature of the input variables are mechanical2 and electrical for the output variables. The piecewise linear capacitance data extracted from the FE simulations is implemented as a two-port model. This biport behaves like a transducer converting the displacement of the seismic mass of the accelerometer into a capacitance. The piecewise linear capacitance data is visible in the *init* statement of the relational (analog) architectural declaration of table III. A space period function of the capacitance versus the displacement enables to define the lookup table over one period. The variable capacitance is periodic to a good approximation due to the high number of electrode

```
ENTITY hrm IS
 PIN (inp, inp0: mechanical2);
END ENTITY hrm;

ARCHITECTURE bhv OF hrm IS
 STATE dn: analog_vector(0 TO 0); STATE dd: analog_vector(0 TO 2);
 VARIABLE dout, lhs, rhs: analog; STATE fout: analog;
 CONSTANT nn, nd: integer;        CONSTANT prop, F: real;
 CONSTANT coefn : real_vector (0 to 0);
 CONSTANT coefd : real_vector (0 to 2);
BEGIN
 RELATION
  PROCEDURAL FOR INIT =>
   NULL;
   F := 1.0; nn := 0; nd := 2; coefn(0) := 1.0;
   coefd(0) := 1446442060.7976346; coefd(1) := 478.76782130605818;
   coefd(2) := 1.0; prop := 240393.2777765124;
  PROCEDURAL FOR DC, AC, TRANSIENT =>
   lhs := coefn(0) * fout; -- build LHS (force)
   dn(0) := fout;
   IF nn > 0 THEN
    FOR i IN 1 TO nn LOOP
     dn(i) := ddt(dn(i-1));  lhs := lhs + coefn(i)*dn(i);
    END LOOP;
   END IF;
   dout := [inp0,inp].d;   -- build RHS (displacement)
   rhs := coefd(0) * dout;   dd(0) := dout;
   IF nd > 0 THEN
    FOR i IN 1 TO nd LOOP
     dd(i) := ddt(dd(i-1));  rhs := rhs + coefd(i)*dd(i);
    END LOOP;
   END IF;
   [inp0,inp].f %= fout;  -- define mech. impedance
  EQUATION (fout) FOR DC, AC, TRANSIENT =>
   (prop/F)*lhs == rhs;
 END RELATION;
END bhv;
```

TABLE I
HDL-A model listing of the mechanical part of the accelerometer.

segments (around 400).

Digital synchronization is used to ensure accurate piecewise behavior of the model (process declaration). The digital architectural declaration is presented in table II. Synchronization is required to force the circuit simulator to calculate a convergence point at each node of the capacitive lookup table to prevent rounding-off errors and allow efficient simulation without having to reduce the maximum time step parameter. For a slowly varying input (displacement of seismic mass), few synchronization steps will occur. When rapidly strong and varying external acceleration is present, as many time steps as needed are calculated. The active *slice* in the lookup table is also updated as transitions occur. The capacitive impedance load is only present for *ac* and *transient* simulation modes, as no current flows for a *dc* analysis.

The models of the mechanical and electrical parts of the accelerometer are compiled and introduced, together with models of the front-end sensing electronics, into a netlist for system level simulation. The global performance of the accelerometer system may now be predicted, and the precision optimized by iterating the device simulation, parameter extraction, model generation and system simulation steps.

V. Conclusions

A numerical parameter extractor and model generator interfacing between device (FE) and system (SPICE) si-

```
ENTITY capa IS
  PIN (inp, inp0 : mechanical2; outp, outp0 : electrical);
END ENTITY capa;

ARCHITECTURE bhv OF capa IS
 STATE din, vout, iout, cval : analog;
 VARIABLE d, C: analog_vector (0 TO 20);
 VARIABLE n,sl: integer;
 VARIABLE inf,sup,step: analog;
BEGIN
  PROCESS
  BEGIN
    forever : LOOP
      WAIT ON RISING (din,sup), FALLING (din,inf);
      IF RISING (din,sup) THEN
        IF (sl < (n - 1)) THEN sl := sl + 1;
          inf := d(sl); sup := d(sl+1);
        ELSE
          REPORT "Overshoot" SEVERITY warning;
        END IF;
      ELSIF FALLING (din,inf) THEN
        IF (sl > 0) THEN
          sl := sl - 1;
          inf := d(sl); sup := d(sl+1);
        ELSE
          REPORT "Undershoot" SEVERITY warning;
        END IF;
      END IF;
    END LOOP forever;
  END PROCESS;
```

TABLE II
HDL-A model listing of entity header and digital process of capacitor of accelerometer.

```
  RELATION
    PROCEDURAL FOR INIT =>
      sl := 0; n := 20;
      step := 20.0e-6;
      d(0) := 0.0;C(0) := 2.298e-11;d(1) := 1.0e-6;
      # table intentionally omitted #
      d(20) := 20.0e-6;C(20) := 2.298e-11;
    PROCEDURAL FOR DC =>
       din := [inp, inp0].d; -- accelerometer's displacement
        vout := [outp, outp0].v;-- capacitance's voltage
        WHILE din/step < 0.0 AND din/step > 1.0 LOOP
          IF din < 0.0 THEN din := din + step; END IF;
          IF din > 0.0 THEN din := din - step; END IF;
        END LOOP;
        FOR i IN 0 TO n-1 LOOP
          IF din < d(i+1) THEN
            IF din >= d(i) THEN sl := i; EXIT; END IF;
          END IF;
        END LOOP;
        cval := 0.0; inf := d(sl); sup := d(sl+1);
    PROCEDURAL FOR AC, TRANSIENT =>
      din := [inp, inp0].d;  -- displacement
vout := [outp, outp0].v; -- voltage
WHILE din/step < 0.0 AND din/step > 1.0 LOOP
          IF din < 0.0 THEN din := din + step; END IF;
          IF din > 0.0 THEN din := din - step; END IF;
        END LOOP;
         cval := (C(sl)+((C(sl+1)-C(sl))/
                 (d(sl+1)-d(sl)))*(din-d(sl)));
         IF din < d(0) THEN cval := 0.0;
         ELSIF din > d(n) THEN cval := 0.0; END IF;
       [outp, outp0].i %= iout;
       [inp, inp0].f %= 0.0;
     EQUATION (iout) FOR DC, AC, TRANSIENT =>
        iout == ddt(vout) * cval;
  END RELATION;
END ARCHITECTURE bhv;
```

TABLE III
HDL-A model listing of relational block of capacitor of accelerometer.

mulation levels was presented. A silicon micromachined accelerometer using capacitive detection was simulated and presented. The approach allowed the optimization of the sensitivity of the device. The resultant behavioral model may be used in an analog circuit simulator to perform simulations together with the detection and linearization electronics. Generation of behavioral HDL models of devices characterized using FEs results in rapid system simulation and prevents convergence problems often encountered when coupling different field solvers. The greatest benefits of the methodology and numerical tools are a faster time to market and greatly reduced prototyping costs.

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References

[1] G. Wachutka, H. Pavlicek, T. Fabula, H. Haffner, N. Hey, T. Feudel, and R. Strecker, "CAD Tools for MEMS", *FSRM*, Rue de l'Orangerie 8, 2000 Neuchatel, Switzerland: FSRM, 1994.

[2] Stephen D. Senturia, "CAD for microelectromechanical systems", *International Conference on Solid-State Sensors and Actuators, and Eurosensors IX*, Stockholm, Sweden, 1995.

[3] B. Romanowicz, PhD. dissertation, "Methodology for the Modeling and Simulation of Microsystems", *Institute of Microsystems, Swiss Federal Institute of Technology of Lausanne*, June, 1997.

[4] Selden Crary and Yafan Zhang, "CAEMENS: An integrated computer-aided engineering workbench for microelectro-mechanical systems", *IEEE Micro Electro Mechanical Systems: An Investigation of Micro Structures, Sensors, Actuators, Machines and Robots*, Napa Valley, CA, USA, February, 1990.

[5] Bart Romanowicz, Yannick Ansel, Matthew Laudon, Christian Amacker, Philippe Renaud, Alain Vachoux and Gerold Schröpfer, "VHDL-1076.1 Modeling Examples for Microsystem Simulation", presented at *2nd Workshop on Libraries, Component Modeling and Quality Assurance, accompanying Computer Hardware Description Languages Symposium 97*, Toledo, Spain, 1996.

[6] B. Romanowicz, P. Lerch, P. Renaud, and A. Vachoux, "Modeling and Simulation of Microsystems, an Experience with HDL-A", presented at *Workshop on Libraries, Component Modeling and Quality Assurance*, Nantes, France, 1995.

[7] Gerold Schröpfer, Sylvain Ballandras, Michel de Labachelerie, Pascal Blind and Yannick Ansel, "Fabrication of a new highly symmetrical in-plane-accelerometer-structure by anisotropic etching of (100) silicon", submitted to *Journal of Micromechanics and Microengineering*, 1996.

[8] Yannick Ansel, Bart Romanowicz, Philippe Renaud, Gerold Schröpfer, "Optimisation of a linear capacitive transducer for a silicon accelerometer",accepted for publication in Eurosensor XI, Warsaw, Poland, 1997.