A New Diffusion Algorithm during Oxidation which can Handle Both Phosphorus Pile-Up and Boron Segregation at Si-SiO_2 Interface

Hironori Sakamoto and Shigetaka Kumashiro
ULSI Device Development Laboratories, NEC Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa 229, Japan
Tel:+81-427-79-9927 Fax:+81-427-71-0938 E-mail:h-saka@lsi.tmg.nec.co.jp

Abstract – A new simulation algorithm during oxidation which can handle both the phosphorus(P) pile-up and the boron(B) segregation has been proposed. In this algorithm, an interlayer(IL) is placed at Si-SiO_2 interface in order to have P pile up. The interface is moved according to the Si consumption during a time step and a new interface is generated at the end of the consumed Si region. A region between an old and a new IL is defined as a transition layer(TL). A diffusion equation is solved inside the TL using local effective diffusion constants in order to fully redistribute the impurities. By using this "diffusion in the TL," the P piled up in the old IL may move through the TL and re-piles up into the new IL, and B segregation can be simulated accurately. The V_{th}-V_{sub} characteristics of an actual buried channel pMOSFET which is simulated using the proposed algorithm agrees well with the experiment.

I. INTRODUCTION

It is well-known that P piles up at Si-SiO_2 interface. Recently, Y. Sato *et al.* found that the P pile-up layer exists in the SiO_2 side and that the pile-up layer is etched off together with SiO_2 layer by diluted HF [1]. Based on their results, M. Akazawa calculated V_{th} of pMOSFETs by using an IL pile-up model and reported drastic improvement of its accuracy over the conventional model [2]. However, in their simulation, the oxidation process is substituted by the SiO_2 layer deposition followed by annealing. Such a method cannot handle the movement of either a Si-SiO_2 interface or a P pile-up IL correctly. On the other hand, accurate modeling of B segregation into SiO_2 during oxidation is also important from a view point of V_{th} of MOSFETs. In this paper, a new simulation algorithm for oxidation coupled diffusion which can handle both the movement of the P pile-up layer and the B segregation has been proposed.

II. METHOD

A. Pile-Up Simulation Method during Oxidation

The flowchart of the proposed simulation method is shown in Fig.1, and the variation the 1D structure and impurity profile are shown schematically in Figs.2.a-2.e. First, an initial IL is placed with a native oxide layer topped on the Si substrate (Fig.2.a). Some part of P piles up into this IL during the diffusion prior to the oxidation. Generally, the IL is created with zero initial impurity concentration when a new material is deposited. According to the experimental results by Y.Sato *et al.* [1], IL is assumed to be removed if either one of the adjacent materials is etched off. Second, the interface is moved according to the Si consumption during a time step and a new interface is generated at the end of the consumed Si region (Fig.2.b). A new IL is also placed at the new interface with zero impurity concentration. Here, a region between an old and a new interfaces is defined as a TL. Third, the shape of the SiO_2 and the TL are deformed according to the volume expansion due to the material conversion from Si to SiO_2 occurred in the TL (Fig.2.c). In this model, the visco-elastic model proposed by H. Matsumoto [3] is used. Forth, the impurity diffusion is solved and the P piled up in the old IL re-piles up into the new IL through the TL (Fig.2.d-2.e). Finally, the TL is converted to a SiO_2region. These steps are repeated until the time step reaches to a specified oxidation time as shown in Fig.1.

B. Effective Diffusion Constants in the Transient Layer

In the conventional oxidation-diffusion simulation, a "motion-induced interfacial flux" [4] is used to account for the impurity redistribution caused by the interface movement. However, since the motion-induced interfacial flux is defined only at the Si-SiO_2 interface, the impurity in the TL cannot be fully redistributed when there is any mesh node inside the TL. In the proposed method, a diffusion equation is solved inside the TL as well using local effective diffusion constants D_{TL} in order to completely redistribute the impurity. By means of the "diffusion in the TL", the P piled up in the old (SiO_2-TL) IL may move through the TL and re-piles up into the new (Si-TL) IL. Moreover, the B segregation into the TL can be simulated more accurately than the conventional method even if there are some mesh nodes in the TL.

When Si atoms react with oxygen atoms at the Si-SiO_2 interface, the lattice structure is reconstructed and the impurities at the interface may move easily with the interface. Therefore, the diffusion constant in the TL can be larger than the one in the bulk Si. Therefore, in the proposed method, local effective diffusion constants are used in the TL. Considering the impurity can move as far as $V_{ox} \cdot \Delta t$ on the average during a time step width Δt, the local effective diffusion constant D_{TL} in the TL is modeled as $V_{ox}^2 \cdot \Delta t/6$. Here V_{ox} is the local moving velocity of the

0-7803-3775-1/97/$10.00 © 1997 IEEE.

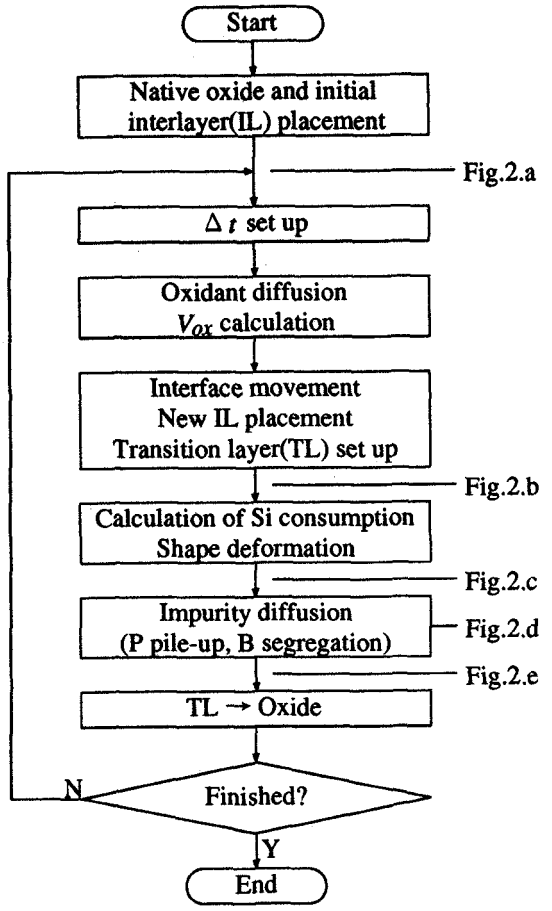

Fig.1: Flowchart of the proposed method.

interface. In the actual simulation, the diffusion profiles is not affected if D_{TL} is set to be larger than $V_{ox}^2 \cdot \Delta t/6$.

III. MODEL PARAMETERS

The transport model proposed by M.Orlowski [5] is adopted to account for the P pile-up. The impurity fluxes in the interface between each region and IL are given by:

Si-SiO_2 interface:

$$J_{\mathrm{Si,IL}} = a_{\mathrm{Si,IL}} C_{\mathrm{Si}} - e_{\mathrm{IL,Si}} C_{\mathrm{IL}},$$
$$J_{\mathrm{SiO_2,IL}} = a_{\mathrm{SiO_2,IL}} C_{\mathrm{SiO_2}} - e_{\mathrm{IL,SiO_2}} C_{\mathrm{IL}},$$

Si-TL interface:

$$J_{\mathrm{Si,IL}} = a_{\mathrm{Si,IL}} C_{\mathrm{Si}} - e_{\mathrm{IL,Si}} C_{\mathrm{IL}},$$
$$J_{\mathrm{TL,IL}} = a_{\mathrm{TL,IL}} C_{\mathrm{TL}} - e_{\mathrm{IL,TL}} C_{\mathrm{IL}},$$

SiO_2-TL interface:

$$J_{\mathrm{SiO_2,IL}} = a_{\mathrm{SiO_2,IL}} C_{\mathrm{SiO_2}} - e_{\mathrm{IL,SiO_2}} C_{\mathrm{IL}},$$
$$J_{\mathrm{TL,IL}} = a_{\mathrm{TL,IL}} C_{\mathrm{TL}} - e_{\mathrm{IL,TL}} C_{\mathrm{IL}}.$$

Here, $e_{\mathrm{IL},A}$ and $a_{A,\mathrm{IL}}$ are the emission and absorption parameters between region A and IL (see Fig.3) and C_A is the concentration of the impurity in region A. The interface transport coefficients and the segregation coefficients can be written in the following way:

$$h_{A,B} = \frac{e_{\mathrm{IL},A} a_{B,\mathrm{IL}}}{e_{\mathrm{IL},A} + e_{\mathrm{IL},B}},$$
$$m_{A,B} = \frac{e_{\mathrm{IL},A} a_{B,\mathrm{IL}}}{e_{\mathrm{IL},B} a_{A,\mathrm{IL}}}.$$

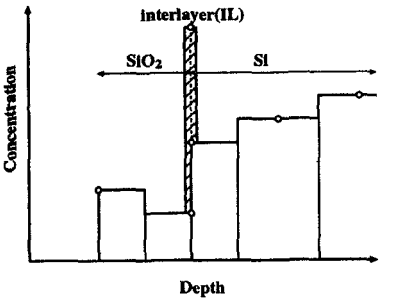

Fig.2.a: Before oxidation

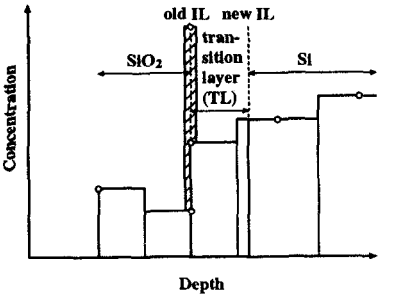

Fig.2.b: Interface movement

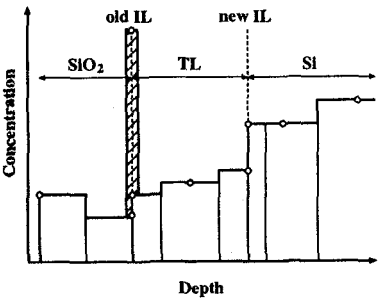

Fig.2.c: Shape deformation

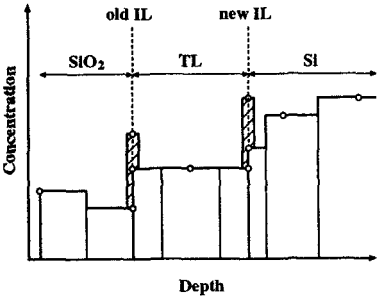

Fig.2.d: During diffusion

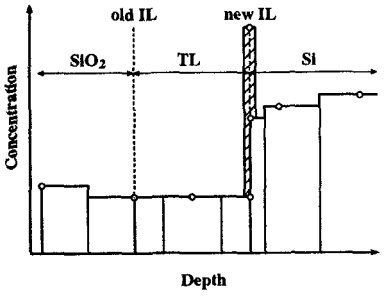

Fig.2.e: After diffusion

Table 1: Model parameters for phosphorus pile-up

	Si-SiO_2(TL) interface		SiO_2-TL interface	
Interface transport coefficient	h_{Si,SiO_2}	$45.42\exp\left(-\frac{1.336eV}{k_BT}\right)$ [cm/min] [7]	$h_{SiO_2,TL}$	0.01 [cm/min]
Segregation coefficient	m_{Si,SiO_2}	30 [6]	$m_{SiO_2,TL}$	1
Absorption coefficient	$a_{Si,IL}$	$0.1333 \cdot h_{Si,SiO_2}$	$a_{SiO_2,IL}$	$h_{SiO_2,TL}$
	$a_{SiO_2,IL}$, $a_{TL,IL}$	$1.333 \cdot h_{Si,SiO_2}$	$a_{TL,IL}$	$h_{SiO_2,TL}$
Emission coefficient	$e_{IL,Si}$	$8.772\exp\left(-\frac{0.7eV}{k_BT}\right) \cdot a_{Si,IL}$ [1]	e_{IL,SiO_2}	$100 \cdot a_{SiO_2,IL}$
	e_{IL,SiO_2}, $e_{IL,TL}$	$0.2924\exp\left(-\frac{0.7eV}{k_BT}\right) \cdot a_{SiO_2,IL}$ [1]	$e_{IL,TL}$	$100 \cdot a_{TL,IL}$
Interlayer width	d_{IL}	5×10^{-8} [cm]	d_{IL}	5×10^{-8} [cm]

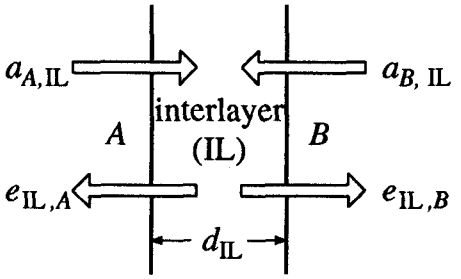

Fig.3: Transport model [5].

The emission and absorption parameters are determined so that the equilibrium segregation and interface transport coefficients between Si and SiO_2 should agree with the experimental results [1,6,7]. The segregation coefficient between bulk Si and IL is determined so that it can reproduce the experimental results of P pile-up reported by Y.Sato *et al.* [1]. The value is:

$$m_{Si,IL} = \frac{e_{IL,Si}}{a_{Si,IL}} = 8.772\exp\left(-\frac{0.7eV}{k_BT}\right).$$

At the SiO_2-TL interface, the interface transport coefficient is set to a value large enough and the segregation coefficient is set to 1 in order to flatten the piled-up P profile. The model parameter values are summarized in table 1.

IV. SIMULATION RESULTS

First, the differences in the P profiles between the proposed (oxidation) and the conventional (SiO_2 deposition + anneal) methods are shown in Figs.4 and 5. Figure 4 shows the time variation of the P concentration at the Si surface when a $1 \times 10^{17}cm^{-3}$ P doped substrate is oxidized at 1000°C in H_2O_2 ambient. If the pile-up model is used, the surface concentration decreases after a short time oxidation due to P pile-up into IL. However, after a long time oxidation, surface concentration recovers and then exceeds its initial value due to P expulsion from the oxidized region (the "snow shoveling" effect). The proposed method can reproduce this effect, but the conventional method fails to reproduce since there is no interface moving.

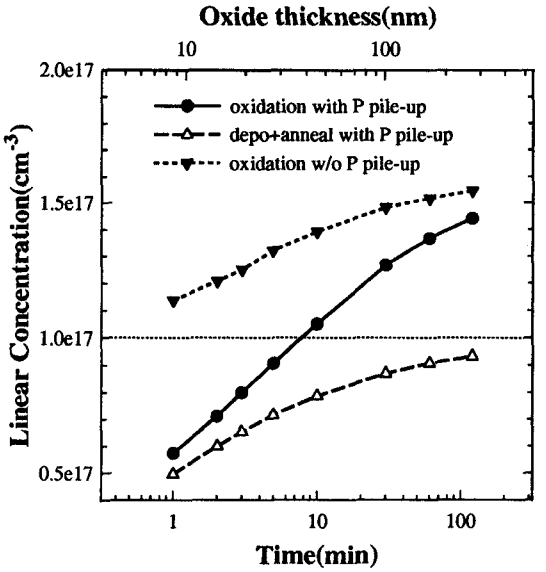

Fig.4: Time variation of P concentration at the Si surface after 1000°C H_2O_2 oxidation of $1 \times 10^{17}cm^{-3}$ doped substrate.

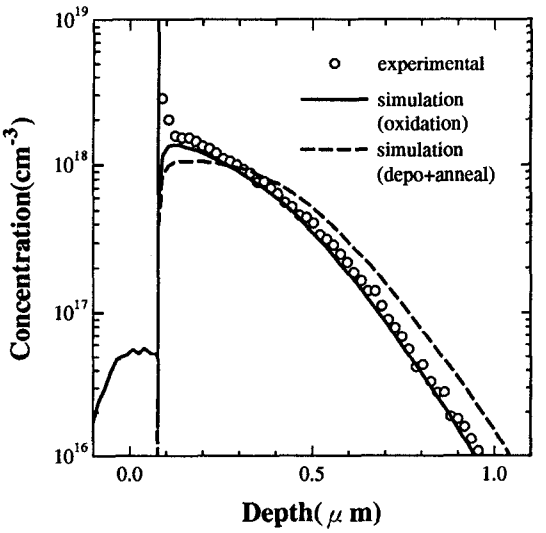

Fig.5: Simulated and measured P profiles after P 150keV $5 \times 10^{13}cm^{-2}$ ion implantation and 1000°C 30min H_2O_2 oxidation.

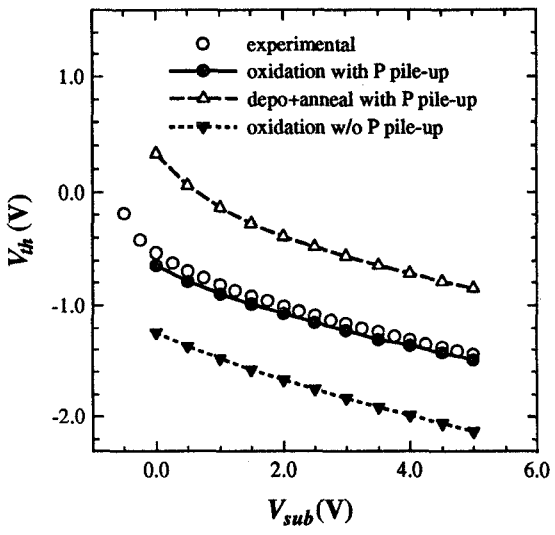

Fig.6: Simulated and measured V_{th}-V_{sub} characteristics of a buried channel pMOSFET.

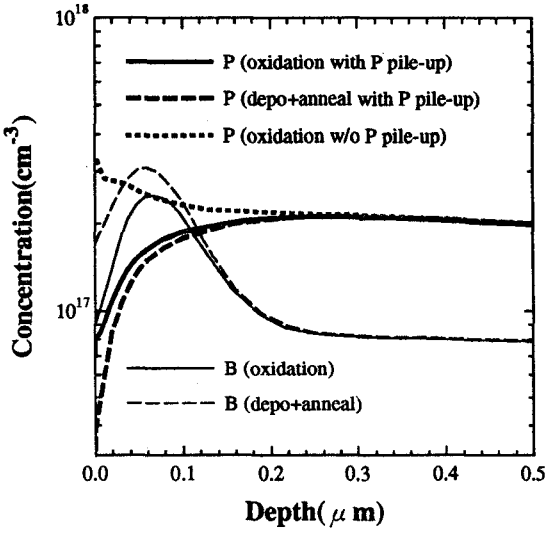

Fig.7: Simulated P and B profiles at mid-channel of a buried channel pMOSFET.

Figure 5 shows simulated and a measured P profiles after implantation and oxidation. Here, the transient and the oxidation enhanced diffusion effects are adjusted to be same between the proposed and the conventional methods. In the conventional method, the absence of the interface movement causes two problems: 1) Decrease in the P concentration near the interface due to no "snow shoveling" effect, 2) Longer P diffusion length due to no interface movement. It is clear that the new method is very effective for accurate P diffusion simulation in the oxidizing ambient.

Next, the simulated and the measured V_{th}-V_{sub} characteristics of an actual buried channel pMOSFET are compared in Fig.6. The simulated P and B profiles at the mid-channel of the same device are shown in Fig.7. If the proposed method is used together with the pile-up model, the simulated V_{th} agrees well with the experiment within 100mV error. However, if the pile-up model is not used, a significant P accumulation in Si causes as much as 700mV error in V_{th}. The conventional method also produces 700mV error in V_{th} even if it is used together with the pile-up model. This is because the segregation of B into SiO_2 during the oxidation is not taken into account. It is clear that the proposed method is very effective for simulating a device fabrication process which contains both P and B.

V. SUMMARY

We have proposed a new simulation algorithm during oxidation which can handle both the P pile-up and the B segregation. This algorithm is characterized by the TL which is defined as a region between Si and SiO_2 and the local effective diffusion constants in the TL. The new method is very effective for accurate P diffusion simulation in the oxidizing ambient and simulating such a device which contains both P and B as a buried channel pMOSFET.

ACKNOWLEDGMENT

The authors would like to thank Dr. S. Asada for his continual support and encouragement. The authors would also like to thank S. Fukai and N. Yamauchi of Mathematical Systems Institute inc. for the software implementation, and N. Sugawara and S. Ohyama for the measurements of the electric characteristics.

REFERENCES

[1] Y. Sato, M. Watanabe, and K. Imai, "Characterization of Phosphorus Pile-Up at the SiO_2/Si Interface", J. Electrochem. Soc., vol.140, No.9, pp.2679-2682, 1993.

[2] M. Akazawa, T. Aoki, S. Tazawa, and Y. Sato, "Phosphorus Pile-Up Model for SiO_2/Si Interface of p-Channel MOSFETs", SISPAD'96, Tokyo, Japan, pp.29-30, 1996.

[3] H. Matsumoto and M. Fukuma, "Numerical Modeling of Nonuniform Si Thermal Oxidation", IEEE Trans. Electron Devices, vol.ED-32, No.2, pp.132-140, 1985.

[4] A. Antoniadis, M. Rodoni, and R. W. Dutton, "Impurity Redistribution in SiO_2-Si during Oxidation: A Numerical Solution Including Interface Fluxes", J. Electrochem. Soc., vol.126, No.119, pp.1939-1945, 1979.

[5] M. Orlowski, "New Model for Dopant Redistribution at Ineterface", Appl. Phy. Lett., vol.55, No.17, pp.1762-1764, 1989.

[6] F. Lau, L. Mazure, Ch. Werner, and M. Orlowski, "A Model for Phosphorus Segregation at the Silicon-Silicon Dioxide Interface", Appl. Phys., vol.A49, pp.671-675, 1989.

[7] K. Sakamoto, K. Nishi, F. Ichikawa, and S. Ushio, "Segregation and Transport Coefficients of Impurities at the SiO_2/Si Interface", J. Appl. Phys., vol.61, No.4, pp.1553-1555, 1987.