A Characterization Tool for Current Degradation Effects of Abnormally Structured MOS Transistors

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Abstract—**A new modeling methodology and an environment for abnormally structured MOS transistors are presented. This methodology uses a three-dimensional device simulator and a curve fitting method to characterize the current degradation effects by extracting the parasitic diffusion resistance from abnormal transistors. We have applied this methodology to 0.5 μm process. Within 5% error, an overall I-V curve fit for various device shapes and bias conditions is achieved. This methodology improves the accuracy of circuit-level simulation.**

I. INTRODUCTION

To reduce the layout size in VLSI circuit design, it is necessary to use some abnormal transistors with irregular source/drain contacts, polygonal source/drain diffusion areas, and curved gate patterns. As the feature sizes are dramatically minimized, however, it is difficult to consider all of these abnormal shapes on Test Element Group (TEG) to extract MOSFET model parameters for circuit simulation. Thus, design engineers may overestimate the circuit performance in circuit simulation unless the current degradation effects [1-3] from those abnormal transistors are considered. In this paper, we introduce an automatic tool, *MAENAD* (Modeling and Analysis Environment for Normal and Abnormal Devices), which models and characterizes the current degradation effects and reflects them in the circuit simulation stage.

II. MODELING OF CURRENT DEGRADATION EFFECTS

The potential distribution and drain currents of the normal and edge contact type NMOS transistors, whose bias conditions are $V_{ds} = 5\ V$, $V_{gs} = 5\ V$, and $V_{bs} = 0\ V$, are shown in Fig. 1. The gate width, gate length, oxide thickness, and junction depth of these transistors are 7.2 μm, 0.5 μm, 120 Å, and 0.2 μm, respectively. Fig. 1 (a) shows the layouts of these transistors and their current flows. It is obvious that the current of a normal transistor flows from drain contacts to source contacts crossing directly through the gate while the current of the edge contact type transistor flows along the diffusion areas. These facts can be proven by monitoring the potential distributions on the silicon surface as shown in Fig. 1 (b). In the case of the edge contact type, the potential drops

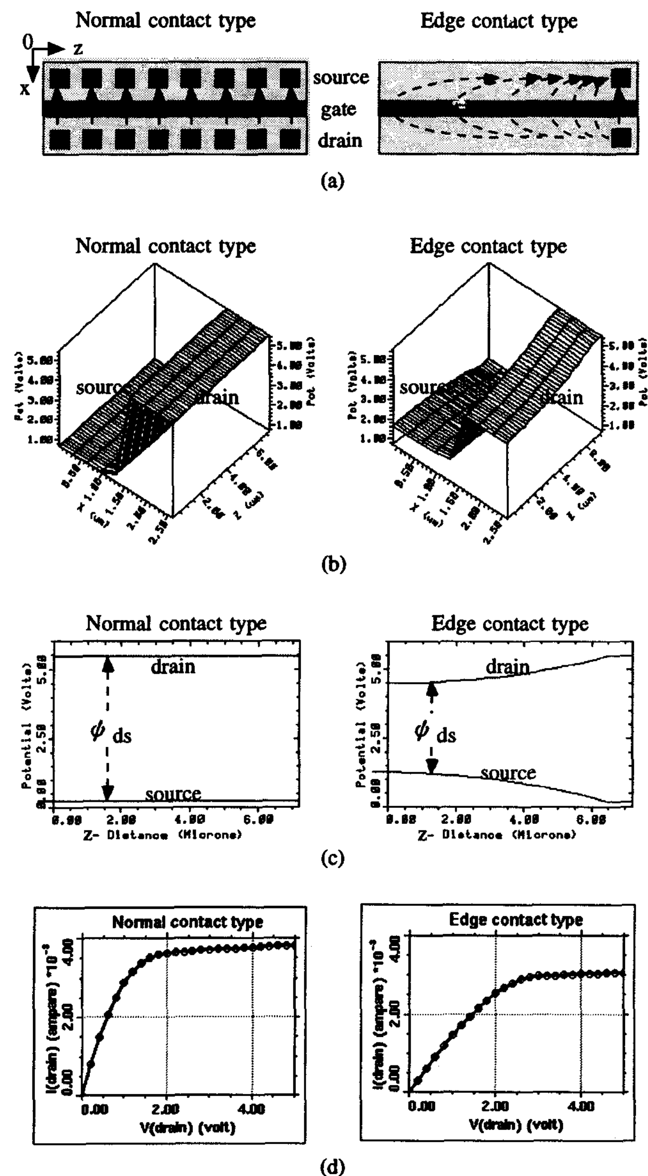

Fig. 1. Comparisons of the potential distributions and drain currents between the normal and abnormal NMOS transistors. (Gate length : 0.5 μm, width : 7.2 μm, contact size : 0.5 μm)
(a) Layouts and current flows of the normal and edge contact type transistors. (b) Potential distributions on the silicon surface for $V_{ds} = 5\ V$. (c) Potential distributions along the source and drain diffusion areas. (d) Drain currents for $V_{gs} = 5\ V$.

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along the current flow line. In Fig. 1 (c), it is shown that the potential drops on the abnormal transistor are due to the diffusion resistance, and that the potential difference (ψ_{ds}) between the source and the drain decreases proportional to the distance from the contacts. Because of these phenomena, the total drain current of the edge type transistor decreases as shown in Fig. 1 (d). In this example, the saturation current of the edge type is 20% smaller than that of the normal one. This current degradation results in bad circuit performance.

The current degradation effects of an abnormal transistor can be modeled by adding the external source and drain resistances to the transistor. The source and drain resistance values are extracted using a curve fitting method (presented in Section III) and the extracted values are added to the MOSFET element card of SPICE as follows;

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Mabnormal nd ng ns nb nmos
+ W = '7.2u + Wdelta' L = '0.5u + Ldelta'
+ RSC = 100 RDC = 100
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Source and drain resistances (R_s and R_d) are specified with *RSC* and *RDC*. W_{delta} and L_{delta} are used to calculate the real geometries of curved gate transistors (Fig. 2). These geometric parameters are simultaneously extracted together with R_s and R_d using the curve fitting method. Like the irregular contact transistors, the current of a U-shaped gate transistor is degraded by the potential drop due to parasitic diffusion resistances. Thus, we can apply the same modeling method to it.

III. Modeling Tool

Fig. 3 shows the structure and the data flow of MAENAD, which automatically characterizes the current degradation effects of abnormal transistors. *Layout & Mesh Editor* generates meshes with layout information and properties of a transistor, such as doping profiles from the two-dimensional process simulation and the oxide thickness. Utilizing this module, the user can specify the efficient meshes for the three-dimensional device simulator (i.e., DAVINCI [4]) to reduce the simulation time. *Main Controller* makes DAVINCI input files of the normal and abnormal transistors with the generated meshes and previously calibrated model coefficients. Then it loads them to *Simulation Engines*, which are high performance workstations containing DAVINCI simulators. Simulation results are stored to *Database*. *Extractor* extracts MOSFET model parameters of the normal transistor using the curve fitting method. It extracts R_s, R_d, W_{delta}, and L_{delta} of the abnormal transistor with the previously extracted parameters also using the curve fitting method. In MAENAD, the Levenberg-Marquardt optimization algorithm is used as a curve fitting method. The results are displayed on *Visualizer* and the extracted parameters are fed back to the post-layout circuit simulation stage. Fig. 4 shows a characterization example of the edge contact type transistor using the graphic user interface of MAENAD.

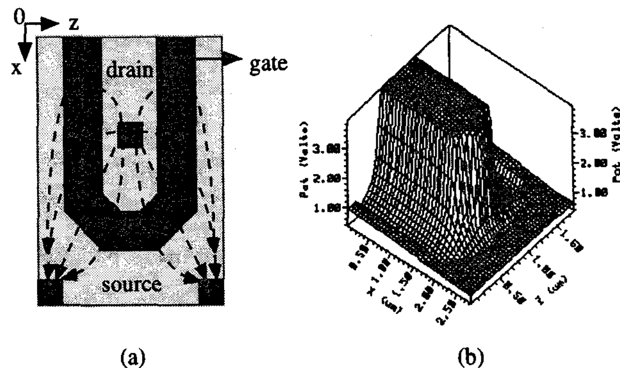

Fig. 2. The current flow and potential distribution of a U-shaped gate transistor (gate length : 0.44 μm, width : 5.0 μm, contact size : 0.28 μm).
(a) Layout and current flow. (b) Potential distribution on the silicon surface.

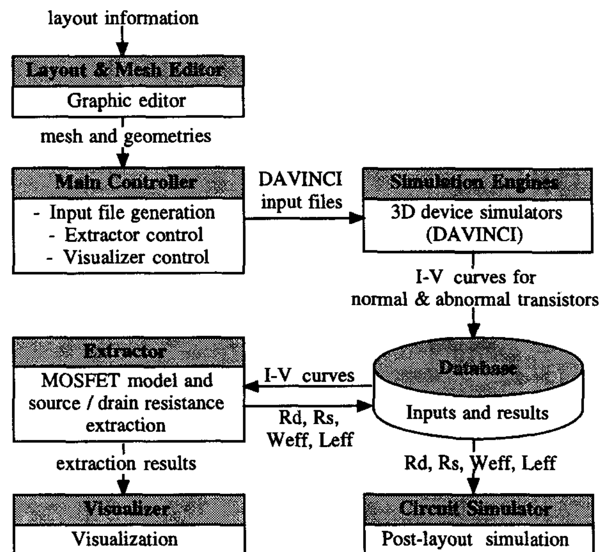

Fig. 3. Structure and data flow of MAENAD.

IV. Application Examples

We have applied this characterization tool to various abnormal transistors, which consist of irregular contacts and polygonal source/drain diffusion areas. All of the simulation results with extracted model parameters and resistance values using HSPICE agree very well with those using DAVINCI (i.e., RMS errors are less than 5%). Fig. 5 shows the fitted curves of the normal and abnormal (center, edge, and diagonal contact type) NMOS transistors whose gate width and length are 7.2 μm and 0.5 μm, respectively. The abnormal transistors have only one contact on source and drain areas. All the current curves

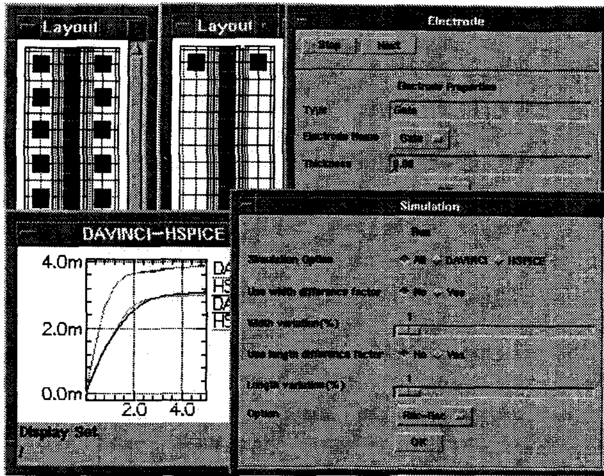

Fig. 4. An example of R_s and R_d extraction using MAENAD.

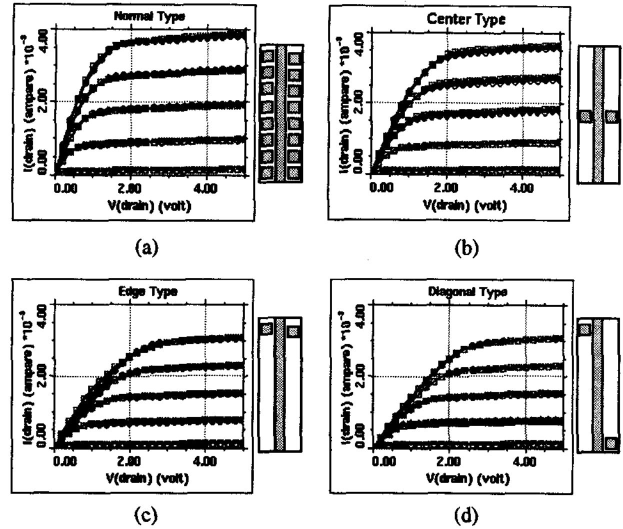

Fig. 5. Modeling results of various irregular contact transistors for V_{ds} : 0 ∼ 5 V, V_{gs} : 1 ∼ 5 V, V_{bs} : 0 V, W=7.2 μm, L=0.5 μm.
(o : curves from DAVINCI, □ : curves from HSPICE)
(a) Normal contact type. (b) Center contact type : R_s=R_d=67 Ω.
(c) Edge contact type : R_s=R_d=136 Ω. (d) Diagonal contact type : R_s=315 Ω, R_d=101 Ω.

show accurate results in both the linear and saturation regions for the various gate bias conditions. Especially, for the center and edge types which contain symmetric contacts, the "$R_s = R_d$" option is used to get the same resistance values. The extracted source and drain resistance values of three kinds of abnormal NMOS transistors are shown in Fig. 5. In addition, we see that the center type is the best pattern to obtain the largest driving current if we can make just one contact each for the source and drain area. Fig. 6 and Fig. 7 show the layouts and extraction results for an NMOS transistor (W/L = 2.6 μm/0.5 μm) and a PMOS transistor (W/L = 4.5 μm/0.5 μm), respectively, which have polygonal source and drain diffusion areas. These results show that the I-V curves obtained from DAVINCI and HSPICE are nearly identical (below 1% RMS error) for both transistors. Therefore, our methodology can be adopted to the transistors which have irregular source and drain shapes.

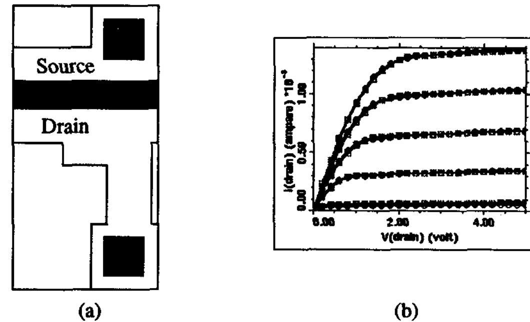

Fig. 6. Modeling results of an abnormal NMOS transistor for V_{ds} : 0 ∼ 5 V, V_{gs} : 1 ∼ 5 V, V_{bs} : 0 V, W=2.6 μm, L=0.5 μm.
(o : curves from DAVINCI, □ : curves from HSPICE)
(a) Layout of an abnormal NMOS transistor. (b) Extraction results : R_s=22 Ω. R_d=287 Ω.

V. Conclusions

MAENAD is an efficient tool to model the current degradation effects of various abnormal transistors using a three-dimensional device simulator and enables designers to obtain very accurate results at the circuit-level simulation.

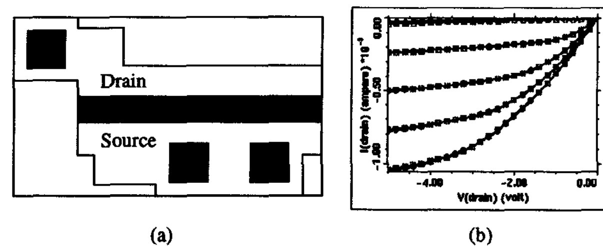

Fig. 7. Modeling results of an abnormal PMOS transistor for V_{ds} : 0 ∼ -5 V, V_{gs} : -1 ∼ -5 V, V_{bs} : 0 V, W=4.5 μm, L=0.5 μm.
(o : curves from DAVINCI, □ : curves from HSPICE)
(a) Layout of an abnormal PMOS transistor. (b) Extraction results : R_s=4 Ω. R_d=697 Ω.

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