Analysis of Channel-Width Effects in 0.3 *um* Ultra-Thin SOI NMOSFETs

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Abstract— **Experiment-based new phenomena, such as LIF energy and channel width effects in ultra-thin (T_{Si} = 700Å) 0.3 *um* SOI NMOSFETs, are analyzed using TCAD tools. The relatively higher doping profile along with the width direction silicon edge can improve the breakdown characteristics (i.e., BV ≅ 9 V at W / L = 0.4 *um* / 0.3 *um*). This effect, which does not coincide with typical BV characteristics in very-small SOIs, is caused by the reduction of the impact ionisation rate due to the doping and geometric effects of the silicon edge as the channel-width becomes narrower. It implies that very small SOI NMOSFETs can be well adopted for the ultra-high density DRAM cells when an optimised doping profile is provided.**

I. Introduction

It is well known that the SOI technology is one of the strongest solutions for the ultra-high density and/or less than 1 V of circuit operation due to its perfect isolation, small junction capacitance, sharp subthreshold characteristics, and excellent latchup immunity [1][2]. However, despite of the recent 16Mb and 64Mb SOI DRAM developments, SOI NMOSFETs suffer from their inherent lower drain-to-source breakdown by the floating body [3][4]. Existing technologies and structures illustrated in Table 1 [5-10] aiming at suppressing the floating body effect (i.e., the source / drain engineering, Ge implantation, and body contacts) are not quite practical in the large volume production because of their process complexity and additional process steps.

II. New Width Effects in 0.3*um* SOI

We have obtained new experimental data for various SOI channel width geometries with respect to the Boron Local Implantation post Field-oxidation (LIF) [4] energies, 60 and 80 KeV. The LIF process is followed after the field oxidation process, such as LOCOS and STI, in order to form a concave doping profile along the silicon thin film.

Fig. 1 shows the measured threshold voltage (Vth) and breakdown voltage (BV) when the channel length and the silicon film thickness are 0.3 *um* and 700 Å, respectively, with regard to various channel widths from 0.4 *um* to 10 *um*. Both BV and Vth are higher at the 60 KeV LIF energy rather than 80 KeV for the channel width of 10 *um*.

Besides, it should be noted that unlikely at 60 KeV LIF, Vth becomes lower at 80 KeV LIF as the channel width reduces from 10 *um* to 0.4 *um*. In addition, BV becomes higher at 60 KeV LIF as the channel width reduces from 10 *um* to 0.4 *um*, while it is constantly low at the 80 KeV LIF. For W / L = 0.4 *um* / 0.3 *um*, a typical geometry in beyond 64Mb DRAM cells, its BV increases by more than 9 V at 60 KeV LIF. This is crucial because it implies that the parasitic bipolar-induced breakdown effect due to the floating body can be effectively eliminated in the very narrow-channel width SOIs only if an optimized doping profile is given. It also indicates that a very small SOI NMOS can be well adopted for the ultra-high density DRAM cells.

III. Simulation and Analysis

To analyze the LIF energy effects, two-dimensional process and device simulators were introduced and calibrated for the structure of W / L = 10 *um* / 0.3 *um*, where the narrow-width effect does not exist, as shown in Fig. 2. In Fig. 3, the simulated Vth values using a two-dimensional device simulator [11] are 1.23 and 1.12 V for 60 and 80 KeV LIF energies, respectively. These values agree well with the measured results for W = 10*um*, 1.21 and 1.11 V for 60 and 80 KeV LIF energies, respectively.

To analyze the narrow width effect, however, it is necessary to introduce a three-dimensional device simulator [12] because just a two-dimensional simulator cannot consider the doping variations along the width-direction. Accordingly, width direction structures were constructed for 60 and 80 KeV LIF energies, as shown in Fig. 4 (a), and expanded into the channel length direction to form a complete NMOS of W / L = 0.4 *um* / 0.3 *um*. Simulated Vth values using the three-dimensional simulator are 1.20 and 0.89 V for LIF 60 K and 80 KeV, respectively, which match well with the measured data (i.e., 1.18 and 0.85 V as shown in Fig. 5 and Table 2).

The Vth difference mainly comes from the relatively lower doping concentration at the silicon film edge compared to the center region because Boron atoms out-diffuse from the silicon edge toward the field oxide. As a result, the conduction channels are induced first along with the film edge relative to the center region. The doping profile at the Si film for 80 KeV LIF condition is lower than that for 60 KeV LIF as plotted in Fig. 4 (b), so that the

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punch-through and the Drain Induced Barrier Lowering (DIBL) effects become more dominant at the silicon edge, resulting in lower Vth as well as lower BV, as shown in Fig. 1.

Secondly, to find out why BV characteristics are improved in narrow width SOI devices when the LIF energy is 60 KeV, simulation structures with channel widths of 0.4, 0.6 and 1.0 *um* and with the same channel length of 0.3 *um* were constructed. Fig. 6 (a) shows depletion shapes and electric field distributions seen from the top along the drain-to-substrate junction for channel widths of 0.4 *um* and 1.0 *um*, respectively. Note that the depletion width is wider and the electric field is lower at the silicon edge adjacent to the field oxide in both structures. This is caused by the lower doping concentration and electric-field effect of the field oxide.

The BV improvements are explained by the following two reasons.

One is the impact ionization rate (IIrat), the main factor that brings about the parasitic bipolar induced breakdown. IIrat at the channel edge is much lower than that of the center because it varies exponentially as a function of the electric field. IIrat can be expressed by [13]

$$II_{rat} = \alpha_{n,ii} \cdot \frac{|\mathbf{J_n}|}{q} + \alpha_{p,ii} \cdot \frac{|\mathbf{J_p}|}{q} \qquad (1)$$

where $\alpha_{n,ii}$ and $\alpha_{p,ii}$ are the electron and hole ionization coefficients, and $\mathbf{J_n}$ and $\mathbf{J_p}$ are electron and hole current densities. Several forms of ionization coefficients have been proposed and the most commonly used is

$$\alpha_{ii} = A_i \cdot exp(-\frac{B_i}{\mathbf{E}}) \qquad (2)$$

where A_i and B_i are the impact ionization constants and $\mathbf{E}$ is the electric field component in the direction of current flow. Moreover, the width portion of both sides of the lower electric field regions marked as 'edge' in Fig. 6 (a) becomes comparable to the 'center' when the channel width is 0.4 *um*. As a result, an average IIrat becomes lower in the narrow width devices [14], as depicted in Fig. 6 (b). IIrats are 1.8×10^{19}, 5.3×10^{20}, 1.3×10^{21} $pairs/cm^3/s$ for channel widths of 0.4, 0.6, and 1.0 *um*, respectively.

The other is that the floating body effect can be reduced and the gate controllability is improved as the width-direction depletion regions from both silicon edges encounter each other, as reported by Hieda [15]. As a result, the hole density of a unit width generated by the impact ionization is much lower in the narrow width device so that the typical parasitic bipolar-induced breakdown is eliminated, which agrees well with the experiments.

IV. Conclusions

New phenomena, such as the LIF energy and channel width effects in ultra-thin SOI NMOS, are analyzed using two- and three-dimensional device simulation. Throughout this work, it is proved that the relatively higher doping profile (i.e., at 60 KeV LIF) at the width-direction silicon edge improves BV characteristics. In addition, the impact ionization rate becomes lower at the narrow width due to the doping and geometric effects of the silicon edge. Therefore, it is concluded that a well optimized channel profile eliminates the parasitic bipolar effect in very small geometric SOI NMOS devices.

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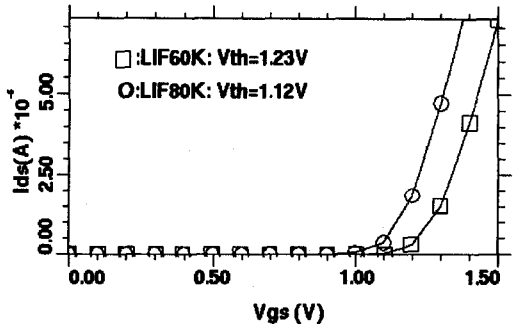
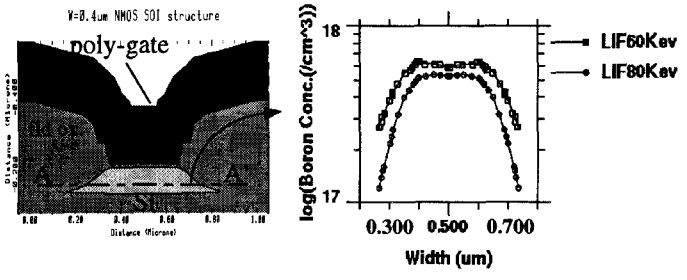


Fig. 3. Simulated Vth's using a 2D device simulator for 60 and 80 KeV LIF energies. Simulated Vth's are 1.23 and 1.12 V for 60 and 80 KeV LIF, respectively, matching well with measured Vth's, 1.21 and 1.11 V (W = 10 μm).



(a) (b)

Fig. 4. A width-direction vertical structure (W / L = 0.4 μm / 0.3 μm) for 3D device simulation to verify LIF energy effects. (a) The width cross section. (b) Boron concentrations along the width-direction cut line (A-A'). Note that the silicon edge profile is lower than that at the center because of out-diffusion of Boron toward the field oxide.

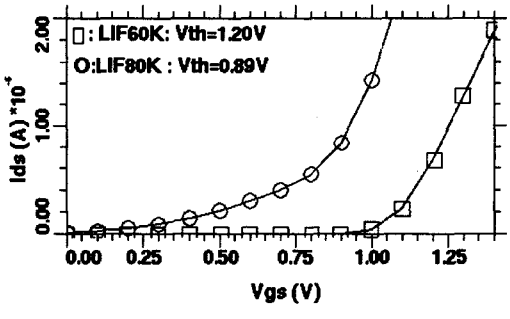
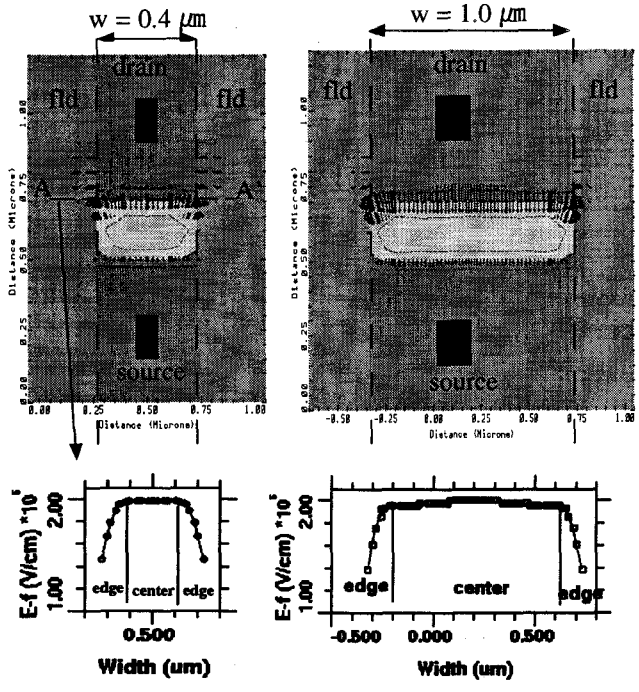


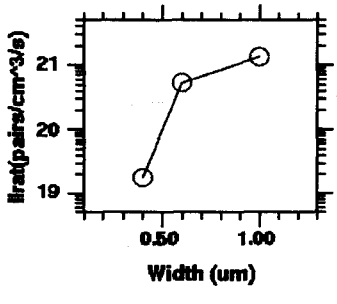
Fig. 5. Simulated Vth's using a 3D device simulator for W / L = 0.4 μm / 0.3 μm. Simulated Vth's are 1.20 and 0.89 V at 60 and 80 KeV LIF, respectively, matching well with the measured data (i.e., 1.18 and

Table 2. Vth comparisons between measured and 2/ 3D simulation values for 60 and 80 KeV LIF energies.

	W/L=10 μm/0.3 μm		W/L=0.4 μm/0.3 μm	
	Measured	2D Sim.	Measured	3D Sim.
LIF 60KeV	1.21 V	1.23 V	1.18 V	1.20 V
LIF 80KeV	1.11 V	1.12 V	0.85 V	0.89 V



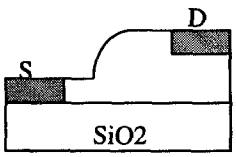
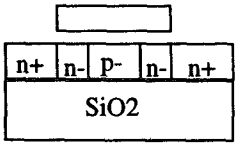
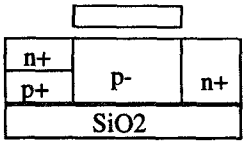
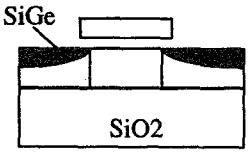
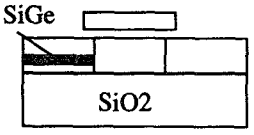
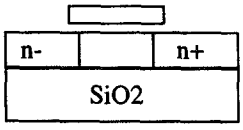
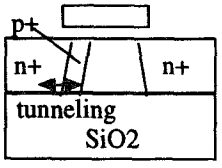
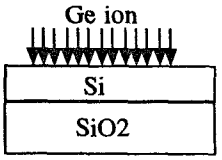
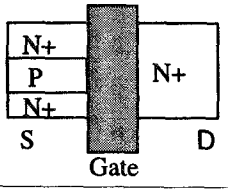
(a)

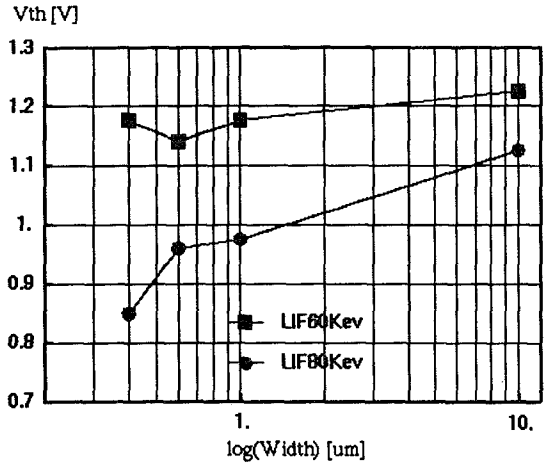


(b)

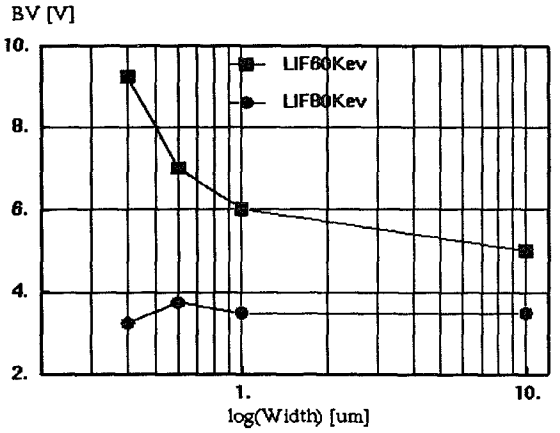
Fig. 6. SOI width effects for Vgs = 0 and Vds = 2.0 V. (a) Depletion shapes and field distributions seen from top (upper) and E-field distributions (A-A') along the drain-to-substrate junction(lower) for W = 0.4 μm and W = 1.0 μm. (b) The average generation rate by impact-ionization for width = 0.4, 0.6 and 1.0 μm.

Table 1. SOI technologies to overcome the parasitic bipolar-induced breakdown effects

Technologies	Structures
Partially Thickened Silicon films on insulator (PTS) : Toshiba [5]	
Gate-Overlapped LDD : Mitsubishi [6]	
Dual Source SOI MOSFET (DSFET) : Toshiba & Stanford	
Ge implanted SOI : Toshiba [7]	
Narrow Bandgap Source (NBS) SOI : Samsung [1]	
Lightly Doped Source (LDS) : U. of Florida [8]	
Self-Aligned Source-Body Contact : UCLA [9]	
Lifetime kill technique : MIT [10]	
Source Region Body Contact [7]	



(a) Vth



(b) BV

Fig. 1. Measured data with 60 and 80 KeV LIF energies for various channel widths (L = 0.3 μm). (a) Vth. (b) BV.

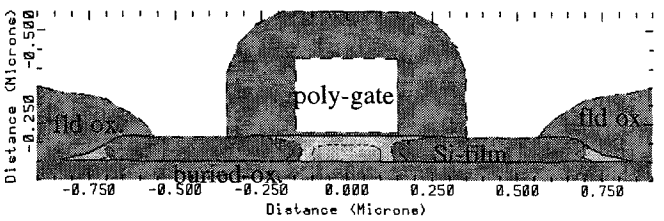


Fig. 2. The vertical structure of a very-thin film partially depleted SOI NMOS (L = 0.3 μm, Tsi = 700 Å) .