Application of TCAD to Designing Advanced DRAM and Logic Devices

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Abstract— **Typical aspects of applying TCAD to designing advanced DRAM and Logic devices are presented focusing on transistors. For prediction at the start of developing new devices, global models which fit marginally to varieties of transistors are used. After preliminary experiments of the new devices, model parameters are best fit to the experimental results using local parameter extractions. These local models are used for process optimization of the devices under development. Response surface models are extensively used with additional information of weighted optimization and statistical analysis. Fast and compact contributions to circuit design are promised by response surfaces of SPICE parameters. A new concept of response surface chains(RSC) is introduced to make the best use of simulated results. Support of TCAD tools to this concept is a key technology for con-current and real-time development of the advanced devices.**

I. Introduction

Advanced DRAM and Logic devices requires sophisticated designing solutions for process, device and circuit optimization problems. Basic reasons are classified into four points:

(a) size effects of device scaling down;

(b) process complexity and severe cost reduction;

(c) device complexity toward high yield and low power;

(d) circuit complexity toward system on silicon such as embedded DRAM;

One of the answer to such problems is using TCAD as a solution tool[1]. In the development of advanced devices, usage of TCAD system can be classified into four phases:

(1) Rough determination of process conditions;

(2) Local modeling to get higher accuracy;

(3) Extensive process optimization;

(4) Contributions to circuit design;

Necessary TCAD tools are different depending on these phases. In this paper, these phases are discussed in more detail from a practical point of view in developing advanced DRAM and Logic devices. Discussions are focused especially on transistors where TCAD offers the best contributions now. Various expansions of response surface models(RSM's) contribute substantially in phase (3) and (4). TCAD system supporting variety of response surface expansions is a key technology for development of advanced LSI's.

II. Rough Determination of Process Flow and Conditions

At the initial stage of developing new process generations or shrinking certain process technologies, TCAD is used for rough determination of process flow and process conditions. In developing DRAM and Logic devices, this phase corresponds to the designs of well, isolation and drain regions. Process conditions for these regions are determined by evaluating several electrical characteristics such as depletion layer widths, threshold voltage of field MOS transistors, drain breakdown voltage and so force. Process conditions of implantation and annealing should be determined roughly at this stage prior to the first experimental lot. However, required accuracy of TCAD at this stage is not severe and so called 'global models' which fit marginally to varieties of former transistors are used. In addition, number of parameters and target characteristics for optimization is not so large. TCAD tool requirements at this stage is thus not so highly sophisticated, and conventional systems[2] still contribute there.

III. TCAD Parameter Extraction

Because of severe device/circuit specification and their trade-off relationship, and of rigorous limitations to fabrication costs, further optimization is highly required in the middle stage of developing advanced DRAM and Logic devices. For such purposes, better accuracy is strongly required to TCAD than in the initial developing stage. A simple solution for this problem is to use measured data from early experiments of the device and to interpolate and extrapolate them efficiently by using TCAD, process and device simulators. This interpolation and extrapolation information is effectively generated by fitting TCAD model parameters directly to electrical characteristics of the device in the local process window. This approach is called 'local modeling' and becomes one of the key technologies in using TCAD systems[3].

The features of local modeling in comparison to so called 'global modeling' are as follows:

(1) Model parameters are fitted to set of transistors with dependence of channel length and other process conditions;

(2) Required accuracy is very high;

(3) Modeling should finish in short term;
(4) Fundamental physics is not discussed in detail;

Typical threshold voltage characteristics fitted to gate length dependence of measured data are shown in Fig.1. This calibration procedure consists of several trials of automatic parameter extractions taking one or two days in total work which is a reasonable time for the next process optimization. Threshold voltage for several process conditions including reverse short channel effects are rigorously described by the local model. Overall errors are below 0.02 volts which are sufficient for the process optimization purposes.

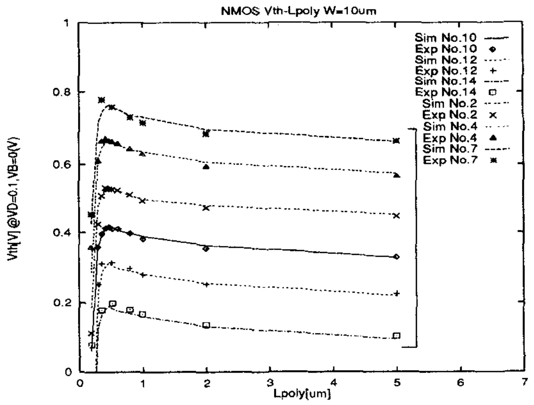

Fig. 1. An example of locally fitted characteristics of nMOSFETs. Threshold voltage of several transistors of process conditions are well fitted including their reverse short channel effects.

In case that large discrepancies exist between measured data and simulated results with default model parameters, the inverse modeling technique[4] helps to determine initial parameters by offering detail information of impurity profile Channel impurity depth profile of a p-channel MOSFET extracted by the inverse modeling technique is shown in Fig.2. In the figure, assumed 'initial' profile is fitted to 'original' profile, and 'result' represents the extracted profile. Such technique give fast information of real profile which helps the determination of initial model parameters for local modeling.

IV. Process Optimization

In advanced sub-micron devices, trade-off relationship causes substantial limitation to device performance, and process optimization becomes more important and difficult. In case of MOS transistors, optimization should be applied to threshold voltage, driving currents, off leakage currents, drain breakdown voltage, hot carrier effects and so on. For process parameters, process conditions for well formation, isolation, channel impurity(shallow and deep), drain impurity(lightly doped drain, pocket implantation), oxide thickness, gate length should be optimized for these characteristics.

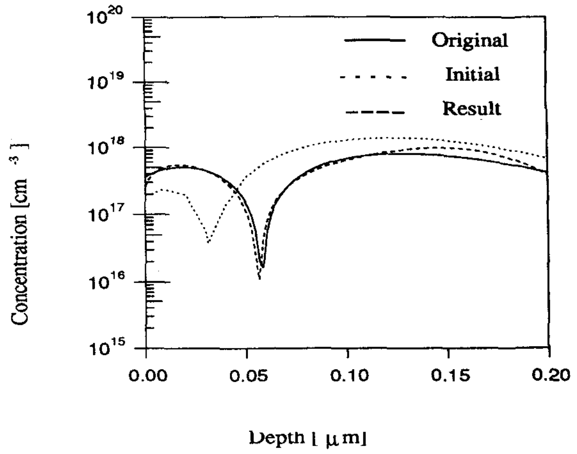

Fig. 2. One-dimensional impurity profile along the depth of pMOS channel. By using Vth-Vb relationship, such depth profile is extracted without making specific device samples for SIMS measurement[4].

TABLE I
Requirements to MOS Transistors in DRAM and Logic.

	Requirements
DRAM side	Low Leakage Current
	High Oxide Breakdown Voltage
	High Hot Carrier Reliability
Logic side	High Driving Current

At this stage, optimization is complicated as follows:

(1) Number of process parameters and target characteristics is large. Problems are high-dimensional;
(2) Requirements to transistors in embedded DRAM are different between DRAM and Logic blocks. Effects of optimization weight should be considered(Table I);
(3) In sub-quarter micron devices, influence of process fluctuation becomes serious. Statistical analysis should be simultaneously considered in optimization;

In the following subsections, multi-dimensional optimization, effects of optimization weight and statistical consideration are discussed with examples.

A. Simple Multi-Dimensional Optimization

Multi-dimensional optimization problems are commonly solved by TCAD system. For instance of DRAM transistors, leakage current and driving current should be optimized to be low and high respectively. TCAD simulations are performed according to design of experiments(DOE) changing process conditions. All results are summarized into response surface models(RSM's)[5] which is a set of numerical functions representing relationship between process conditions and device characteristics. Simultaneous optimization of several device characteristics is then reduced to a numerical problem on RSM's. Minimizing summation of normalized errors is a simple task for modern computer science. Such simple RSM's are commonly used in modern TCAD systems.

B. Response Surface Considering Optimization Weight

As mentioned above, requirements to MOS transistors are different by their usage. It is not enough to have a simple optimization tool using RSM's when all the desired characteristics are not fulfilled at once. In this case, device designers consider the total performance of circuits and try different optimization weight values to get good balance of several characteristics[6]. Here, we have introduced a concept of response surfaces on optimization weight(RSOW's) which are response surfaces of optimized points of both parameters and targets, as functions of optimization weight values.

An example of RSOW of saturation current(I_{Dsat}) of MOSFET's is shown in Fig.3. The system automatically changes the optimization weight and optimization is automatically performed for each set of weight values. After all, new response surfaces on optimization weight values are obtained. The concept of RSOW provides a substantial freedom and speed-up of optimization decision to device designers.

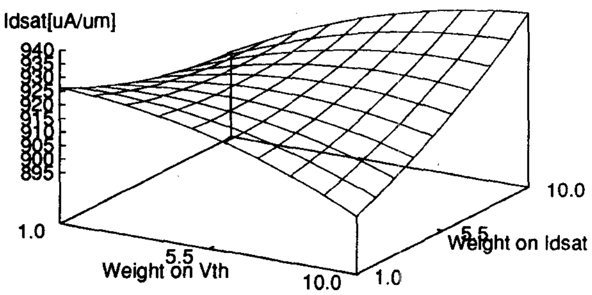

Fig. 3. An example of response surface on weight(RSOW) of saturation current (I_{dsat}) as a function of optimization weight on threshold voltage(V_{th}) and I_{dsat} itself.

C. Response Surface Considering Statistics

Another difficulty of device designers is to consider effects of process fluctuation on target characteristics. For such purposes, statistical analyses using response surfaces are efficient. We use simple Monte Carlo calculation on the response surfaces to get response surfaces of standard deviation(σ). Fig.4 shows σ of threshold voltage as a function of channel dosage and oxide thickness. After getting such response surfaces of standard deviation(RSSD), device designers can easily optimize target functions and their unstability on the same level.

Statistical analysis is also important from another point of view which is process margin. For this purpose, a concept of response surface from σ to σ (RSSS) is useful. Fig.5 shows an example of RSSS, response surface

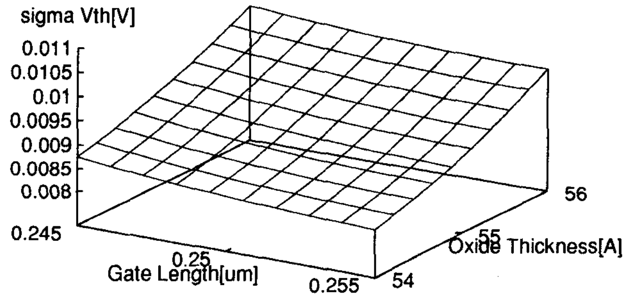

Fig. 4. An example of a response surface of standard deviation(RSSD) of threshold voltage as a function of gate length and oxide thickness. The standard deviation is calculated through Monte Carlo calculations on the original response surface of the threshold voltage.

of $\sigma_{I_{Dsat}}$ as a function of σ_L. RSSS can be derived from original response surface model(RSM) without additional simulations.

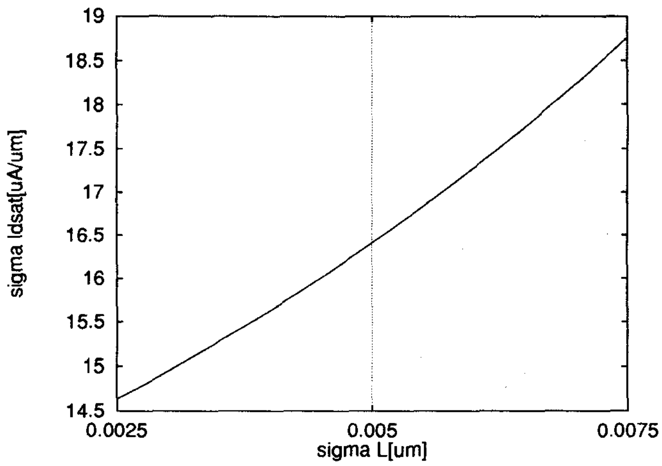

Fig. 5. An example of response surface between σ_L and $\sigma_{I_{dsat}}$(RSSS). Such information is useful for process control.

V. Contributions to Circuit Design

Circuit design of advanced devices requires more device knowledge such as 3-dimensional effects, parasitic effects of layout, temperature dependence, and effects of process fluctuations(Table II). For such purposes, accuracy of SPICE models is insufficient when model parameters are varied to see effects of process conditions. Such inaccuracy of the model limits circuit optimization of advanced LSI's, and compact and accurate tools are highly required.

A concept of response surface of SPICE parameters(RSSP) is recommended as the best tool for such purposes. Circuit designers use SPICE as it is with process dependent SPICE parameters. To show the effectiveness

TABLE II
Objectives of Circuit Simulation
and TCAD Contributions.

	Objectives	TCAD contributions
Logic side	Transistor Size	Parameter Prospection
	Layout Parasitics	3D LCR analysis
	Temperature margin	Parameter Prospection
DRAM side	Process Fluctuations	Parameter Sensitivity

of this approach, propagation delay time(t_{pd}) analyzed by two approaches are compared in Fig.6. Dashed and solid lines are obtained by giving fluctuation to SPICE parameters and to process conditions respectively. The latter approach contains all information of cross-term effects between process and SPICE parameters which are lost in the former approach. RSSP approach provides more accurate prospection of circuit performance and its margin.

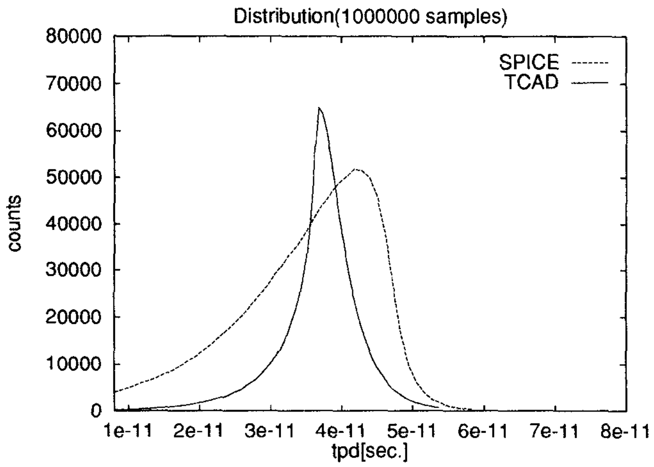

Fig. 6. An application of response surface of SPICE parameters(RSSP). Propagation delay time(t_{pd}) is derived by two different ways, SPICE based(dashed line) and TCAD based(solid line).

VI. TCAD System for Response Surface Chain

As discussed in prior sections, TCAD applications to process optimization and circuit design need some variations of RSM, RSOW(RS on optimization weight), RSSD(RS of standard deviation), RSSS(RS between σ and σ) and RSSP(RS of SPICE parameters). Derivation of these expansions of response surfaces does not spend long calculation time because it is obtained by simple analytical calculations without additional simulations. TCAD tool supporting such response surface chains(RSC) is an efficient solution for requirements of development of advanced DRAM and Logic devices(Table III).

VII. Summary

Typical aspects of applying TCAD to designing advanced DRAM and Logic devices are presented. In the initial stage, global models are used to decide rough process conditions. In the TCAD parameter extraction, inverse modeling method helps to get initial parameters, and then automatic parameter extraction is performed referring to the experimental data from early stage of the development. In the process optimization, response surface models are iteratively used, and some new expansions of response surface are introduced. For circuit designers, response surfaces of SPICE parameters are promised technology to introduce maximum productivity with minimum knowledge of TCAD tools. It is highly required to TCAD system to support extensive use of response surface chains in order to make the best use of simulated results.

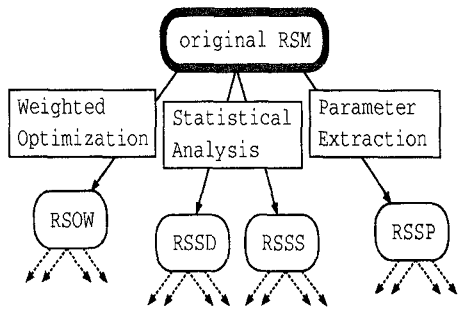

Fig. 7. A schematic representation of the concept of response surface chains(RSC). Only the original RSM is derived by simulations. TCAD system is required to support derivation of such RSC.

TABLE III
Applications of Various Response Surfaces.

	Features	Applications
RSOW	Weight of Optimization	Optimizing embedded DRAM transistors
RSSD	Standard Deviation	Optimizing V_{th} and $\sigma_{V_{th}}$
RSSS	σ to σ	Process Control of $\sigma_{V_{th}}$
RSSP	SPICE Parameters	Process Fluctuation on Performance

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