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An Amorphous-Silicon Thin-Film Transistor Model Including Variable Resistance Effect

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1.Introduction

A circuit simulator which has a device model with the capability of precise description of the electric characteristics of amorphous-silicon thin-film transistors (TFT) is required to efficiently design and analyze liquid crystal display (LCD) panels. The bulk crystalline silicon MOSFET model implemented in SPICE is not suited for TFT's, the characteristics of which are affected by the distributed nature of the localized states. Several modeling approaches, in which the distribution of the states in the energy band gap is taken into account, have already been reported[1],[2]. However, these models cannot accurately predict the performance of devices with different bias conditions or geometries, because of the ignorance of the bias dependent resistivity in the active layer, especially at the source and drain edge. And such behavior of the parasitic resistance is the feature common to inverted staggered TFT's, and it plays an important role in the device modeling. In this paper, a new analytical DC model including the modulation effect of the resistivity is presented, and the accuracy of the model is shown by excellent comparisons with the experimental data .

2.Model

A schematic representation of the equivalent circuit model for the TFT is shown in Fig.1. (R_s+R_{s0}) and (R_d+R_{d0}) denote the source and drain series resistances, where R_{s0}, R_{d0} include the contact component and remain unchanged, and R_s, R_d include the active layer and vary with the external bias conditions. The model description to characterize these variable resistances is derived by the derivative of the current equation for the n-i-n diode model and is given by

$$R_s = R_0/\{R_0 K_x (V_{s''s'})^{1/\alpha} + 1\} \quad (1)$$

$$R_d = R_0/\{R_0 K_x (V_{d'd''})^{1/\alpha} + 1\} \quad (2)$$

$$K_x = qK_0 W L_p \mu_n N_c (1/\alpha + 1)(\varepsilon_s / kg_d T_d)^{1/\alpha} T_{si}^{-(2/\alpha+1)} \quad (3)$$

$$\alpha = T/T_d \quad (4)$$

where R_0 is the intrinsic maximum resistance inserted parallel to the differential resistance; W is the channel width; K_0 is the fitting parameter to correct the two dimensional effect; L_p is the effective length of the diode; μ_n is the band mobility; N_c is the density of the states in the conduction band; q is the electronic charge; ε_s is the dielectric constant of the semiconductor; T_{si} is the thickness of the active layer; g_d is the states distribution; k is the Boltzmann constant; T is temperature; and T_d is the characteristic temperature of the localized states. In the circuit equation, the above (R_s,R_{s0}) and (R_d,R_{d0}) are respectively lumped together, so the internal nodes (S',D') are not generated. And the expression of the non linear current source (I_{ds}) shown in Fig.1, which describes the effect of the distributions of the states and the channel length modulation, is newly developed and has the property of the smooth transition between the different operation regions that is suitable for circuit simulation programs.

3.Results and Discussion

Physical validity of the new model is confirmed by the bias dependence of the source and drain series resistances shown in Fig.2, in which the data, extracted by the method of [3], are plotted against the effective gate drive voltage (V_{gs}-V_{th}) for several values of the drain voltage. The resistance increases at lower gate and/or drain bias due to the smaller voltage drops across R_s and R_d, and gradually approaches the value of (R_0+R_{s0}). In the previous model[2], the n-i-n diode is used as the equivalent current source for the gate length shortening in the saturation region and therefore cannot explain the behavior of series resistance in the small drain bias region.

The measured (diamonds) and calculated (solid lines) I_{ds}-V_{ds} and I_{ds}-V_{gs} characteristics are compared in Fig.3, and very good agreement is found in both the linear and the saturation region through devices with different channel lengths. The parameters necessary to the calculation are optimized by data fitting and summarized in Table.1. The dashed lines shown in Fig.3-2 and Fig.3-4 denote the calculated characteristics using the conventional constant series resistance model as the reference.

4.Conclusion

A new analytical drain current model including variable series resistance for the a-Si:TFT is presented. Results calculated by the model show very good agreement with experimental results for all operating bias conditions and indicate the scalability over different device geometries.

(References)

[1]T.Leroux, "Static and Dynamic Analysis of Amorphous-Silicon Field-Effect Transistors," Solid State Electron., vol.29 No.1, pp.47-58, 1986

[2]M.Hack, M.S.Shur and J.G.Shaw, "Physical Models for Amorphous-Silicon Thin-Film Transistors and Their Implementation in a Circuit Simulation Program," IEEE Trans. Electron Devices, vol.36, No.12, pp.2764-2769, Dec. 1989

[3]K.Terada and H.Muta, "A new method to determine effective MOSFET Channel Length," Japan. J. Appl. Phys., vol.18, No.5, pp.953-959, 1979

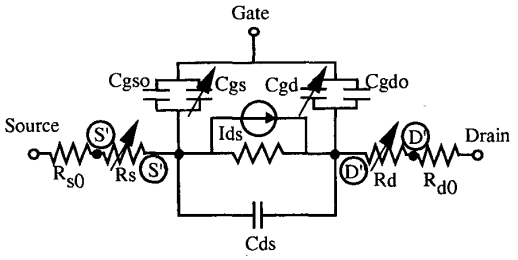

Fig.1 Equivalent circuit description of the presented a-Si:TFT model.

Table.1 Model parameters of the a-Si:TFT.

$R_0 = 4.10\times10^6$ [Ω]	$\mu_n = 2.05\times10^1$ [cm^2/Vs]
$R_s = 1.20\times10^6$ [Ω]	$N_c = 1.04\times10^{19}$ [cm^{-3}]
$R_d = 1.20\times10^6$ [Ω]	$\varepsilon_s = 1.0\times10^{-10}$ [F/m]
$K_0 = 1.0$ [-]	$T_{si} = 1.0\times10^{-7}$ [m]
$L_p = 1.0\times10^{-6}$ [m]	$g_d = 5.0\times10^{18}$ [$cm^{-3}eV^{-1}$]
	$T_d = 1.20\times10^3$ [K]

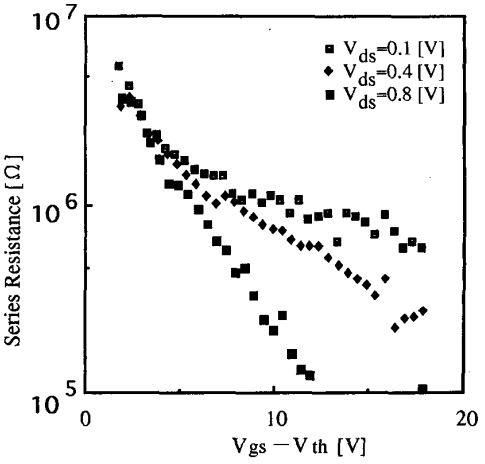

Fig.2 Gate and drain bias dependence of the source and drain series resistance.

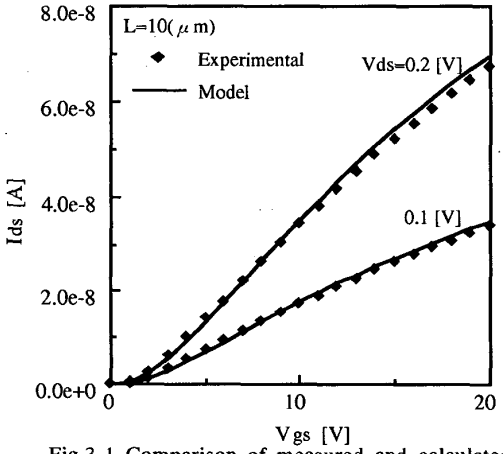

Fig.3-1 Comparison of measured and calculated I_{ds}-V_{gs} characteristics for the 10 μm channel length device.

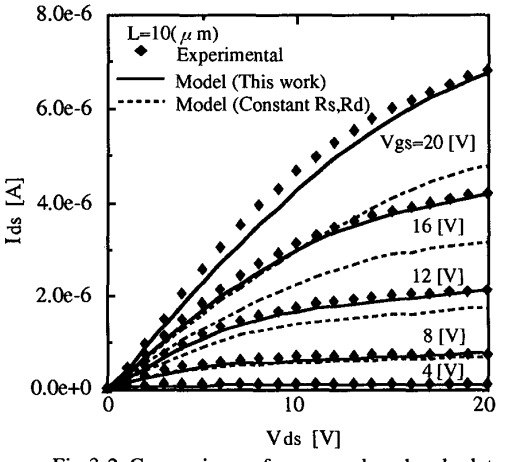

Fig.3-2 Comparison of measured and calculated I_{ds}-V_{ds} characteristics for the 10 μm channel length device.

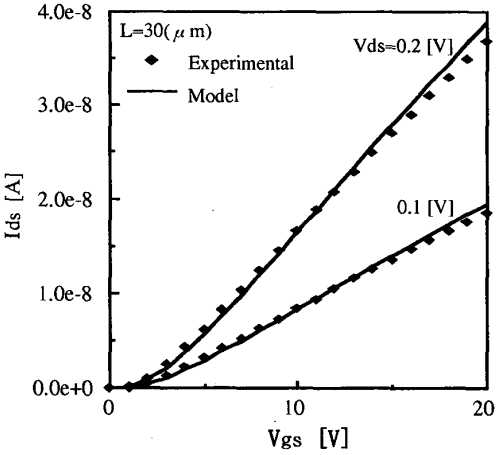

Fig.3-3 Comparison of measured and calculated I_{ds}-V_{gs} characteristics for the 30 μm channel length device.

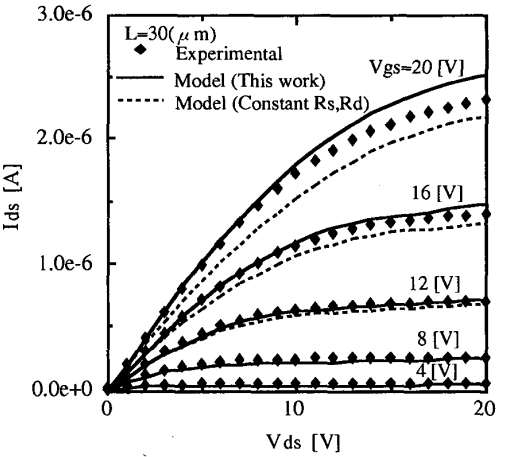

Fig.3-4 Comparison of measured and calculated I_{ds}-V_{ds} characteristics for the 30 μm channel length device.