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A Consistent Dynamic MOSFET Model for Low-Voltage Applications

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The development towards lower voltages and even ultra-low-power (ULP) technologies [1, 2, 3] makes ever higher demands on compact device model accuracy. We present a new approach to dynamic MOSFET modeling, which is especially suited for the simulation of low-voltage mixed analog digital circuits. The model is based on terminal charges and conductive currents which are determined from transient current/voltage data which can be easily obtained through measurement or simulation of the devices.

Model Function and Simulation Environment. The model function is based on a physically motivated interpolation of the terminal currents and charges of the device. The interpolation also supplies the derivatives, i.e., the conductance and capacitance matrices of the device. These data are directly interfaced to a new circuit simulator, MINISIM [4], which uses charge conservative capacitance modeling. The interpolation uses piecewise polynomial and/or exponential splines to account for the physical nature of the quantities (especially the exponential dependence of the currents). This approach rules out common problems like, e.g., discrepancies between the AC-model conductance parameters and the derivatives of the DC-model currents.

Device Characterization. The input data to the model can be obtained either by measurements or by process and device simulations. For this work we used VISTA with MINIMOS [5] to obtain the data by coupled process and device simulation. All conductive currents can be obtained directly from DC measurements. The charge data are computed from transient simulations as shown in Fig. 1 for the case of a two-pole: the device is modeled as a quasi static black box which is equivalent to a nonlinear conductance parallel to a nonlinear capacitance $C(v) = dq/dv$. Applying a symmetrical trapezoidal voltage $v(t)$ to the device will result in a current $i(t)$ which can be separated into a conductive current $i_{cond}(v) = (i(t_1(v)) + i(t_1(v)))/2$ and a capacitive current $i_{cap}(v) = (i(t_1(v)) - i(t_1(v)))/2$ which relates to the charge as $i_{cap}(v) = dq/dt = (dq/dv) \cdot (dv/dt)$. Thus, the charge can be determined as $q(v) = q_0 + \int_{v_1}^{v_2} i_{cap}(v)dv$. The charge offset q_0 can be determined from $q(0) = 0$. In the case of the MOSFET we have a three-pole (assuming the source always grounded), one of the other terminals is ramped, and the currents at all terminals (including the ramped one) are measured and subsequently converted to i/q-data. To obtain a complete field of charge data, including the charge offset, a series of transient measurements/simulations is required as shown in Fig. 2.

According to the desired ranges and step sizes of V_{bs}, V_{gs}, and V_{ds}, one transient in 'V_{bs}-direction', n transients in 'V_{gs}-direction', and $n \times m$ transients in 'V_{ds}-direction' are measured or simulated. Of these, the first $1 + n$ are required for the charge offset computation. The steepness of the ramp determines the accuracy of the charge data and the influence of non-quasi-static effects accordingly. Both can be verified with single transient measurements, using the i/q-extraction software (cf. Fig. 3). For the simulation with MINIMOS the input decks are generated automatically according to the range settings which also control the computation of the current/charge data.

Applications. Example applications are shown in Figs. 4–6. Fig. 4 shows the simulated switching transients of an RS flip-flop designed in a 0.5V ultra-low-power technology [3]. The same technology can be used to build OPAMPs, operating at even lower supply voltages. Due to its inherent accuracy, our new model could show the feasibility of ultra-low-power OPAMPs working at supply voltages well below $1V$. Fig. 6 shows the simulated large-signal step response of the two-stage OPAMP shown in Fig. 5 operating as a follower at $V_{DD} = 0.4$V. The frequency compensation is accomplished by wider output transistors (M7, M8), utilizing their internal capacitances rather than a separate capacitor (C1). The OPAMP is biased for medium speed, consuming a total of 4.0μW.

Conclusion. Our new low-voltage MOSFET modeling approach, together with the supporting software enables the accurate simulation of modern mixed analog digital circuits directly from measured or simulated data. This can be profitably used for process evaluation and optimization on the circuit level without intermediate parameter fitting.

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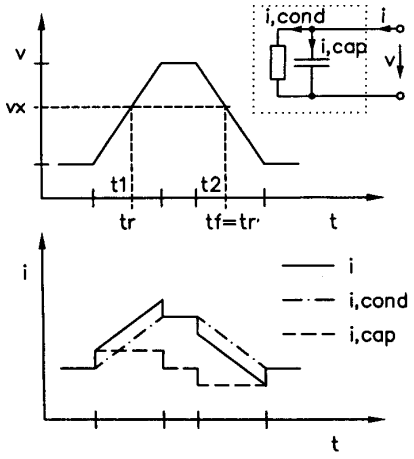

Figure 1: Quasi static black-box model of a two-pole

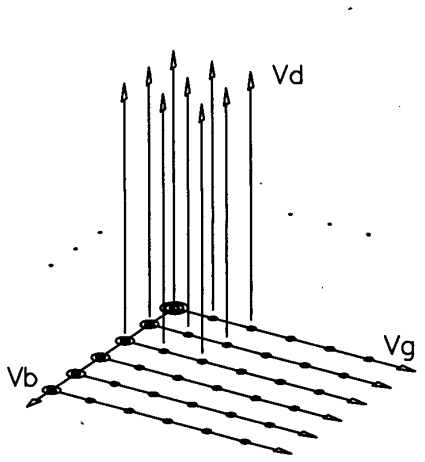

Figure 2: Transient MOSFET simulations / measurements

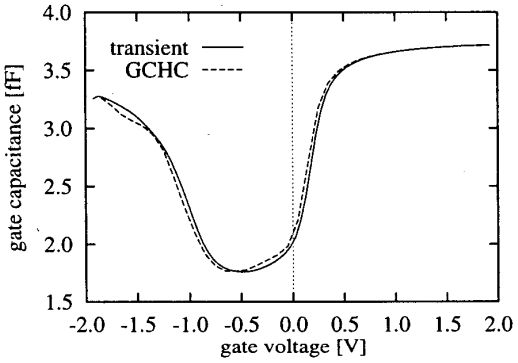

Figure 3: Gate capacitance of an ULP n-channel MOSFET ($V_{ds} = V_{bs} = 0$). - - -: computed through accurate gate charge integration using MINIMOS's 'GCHC' option. ——: transient method ($t_r = 3$ns).

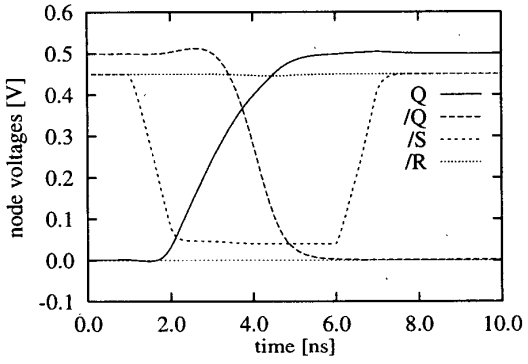

Figure 4: Switching transients of an ULP RS flip-flop ($V_{DD} = 0.5$V)

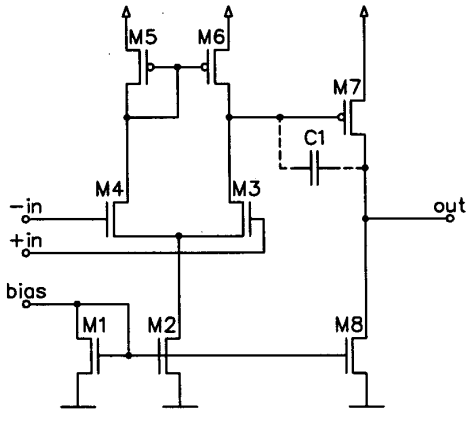

Figure 5: ULP OPAMP with a self-compensating output stage

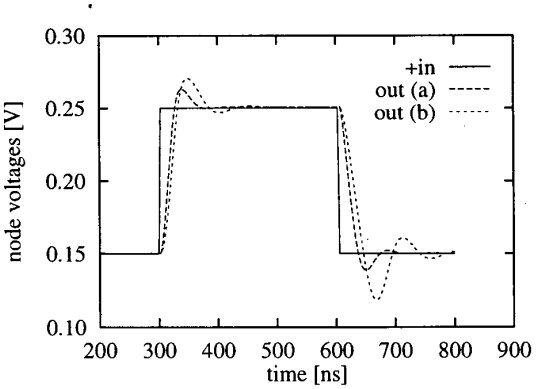

Figure 6: Large-signal step response of an ULP OPAMP operating as a follower at $V_{DD} = 0.4$V with (a) $C_L = 0$pF and (b) $C_L = 1$pF.

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