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A Triangular Mesh with the Interface Protection Layer Suitable for the Diffusion Simulation

Toshiyuki Syo,Yutaka Akiyama,Shigetaka Kumashiro,Ikuhiro Yokota and Susumu Asada
ULSI Device Development Laboratories, NEC Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa 229, Japan
TEL:81-427-79-9927 FAX:81-427-71-0938

Abstract

An automatical Delaunay partitioned mesh generation which is effective in reduction of numerical errors in a diffusion process near the interface or in the thin layer is proposed. An interface protection layer[1] which consists of a rectangular mesh locally conformed to a material interface is introduced. A validity of the interface protection layer for avoiding an artificial threshold voltage shift of about 1 V due to a boron penetration through a pMOS gate oxide is demonstrated.

1.Introduction Ushio et al.[2] showed that numerical errors of the impurity concentration at the boundary increase when a diffusion constant is quite different between two adjacent materials. Figure 1(a) shows simulated boron profiles for various mesh sizes in the oxide. As shown in Fig.1(a) if a coarse mesh is used in the oxide, the impurity concentration of the silicon side decreases. Since a mesh in the oxide layer has a larger control volume than the silicon layer at the interface, more impurity accumulates in the oxide layer than the silicon layer. To reduce this error, they proposed an impurity flux model defined between the two imaginary points at each side of the boundary. However, extension of their method to the higher-dimensional problem is not straightforward. Where to place imaginary points and how to evaluate the interface flux are raised as questions. One method to assure accuracy without introducing any imaginary point is to keep the thickness of the control volume constant and as thin as possible at each side of the interface. However, no previous two-dimensional process simulator can generate such kind of mesh.

2.Method We took advantage of the mesh generation method proposed previously by some of authors[1] with very thin surface protection layer to fulfill the above requirements. In [1], the interface protection layer(IPL) is used to prevent parasitic resistance in the current parallel to the interface. In this paper, a similar method is used to improve the accuracy of diffusion flux vertical to the interface. The method of the mesh generation with an IPL is briefly described below:

1. Generate initial boundary grids and initial bulk grids except the IPL.
2. Generate the IPL from the boundary grids.
3. Connect all grids to achieve a Delaunay partitioning.
4. If triangular mesh whose edges connect the inner grids to boundary grids exists, project vertices of the inner grids on the boundary.
5. Repeat from 2 to 4 until new projection grids do not generate.

Figure 2 shows the mesh with the IPL applied to a trench device. Delaunay partitioned mesh with the IPL can be automatically generated for any arbitrary shaped device in two-dimension.

3.Result Figure 1(b) shows the simulated boron profiles for various mesh sizes in the oxide with the 0.5nm protection layer. In this case, boron profiles near the interface of the silicon side do not depend on the mesh sizes. The above results show the mesh with a 0.5nm IPL is effective for a diffusion simulation, especially each side of the boundary has a quite different diffusion constant.

In addition to that, a following desirable effect is added. Recently, the gate oxide has become thinner in order to achieve a lower operating voltage. With this trend, a penetrated boron through the gate oxide becomes a subject of discussion[3]. When that process with various mesh sizes in the oxide is simulated, the total value of the penetrated boron may differ. Figure 3 shows the simulated boron profiles after a BF_2 ion-implantation on a polysilicon/oxide/silicon structure. A boron diffusion model enhanced by fluorine doses in the oxide[4] is used. In the case of the mesh without the IPL, the boron diffusion through the oxide into the silicon is enhanced significantly. The oxide layer is so thin that the mesh has edges which directly connect the polysilicon/oxide interface to an oxide/silicon interface. If a directly connected edge from one boundary grid to the other one exists, the boron diffuses not by a local concentration gradient but by a difference of the concentration at each interface. On the other hand, in the case of using the IPL, edges which directly connect the polysilicon/oxide interface to the oxide/silicon interface disappear, therefore the boron diffuses normally. This difference of the channel profile causes about 1 V threshold voltage shifts as shown in Fig.4. These results suggest a mesh with the IPL is indispensable for a process simulator as well as a device simulator.

4.CPU-time for the mesh Generation Figure 5 shows the total CPU-time for the mesh generation. Generation time of the mesh with the IPL takes a little more time than the conventional mesh. This is because several times of iterations occur to project vertices of the triangle whose edges are connected to the grids inside of the IPL on the boundary. However, the CPU-time for the mesh generation stays quite small and is $\mathcal{O}(n)$ where n is a total number of mesh elements.

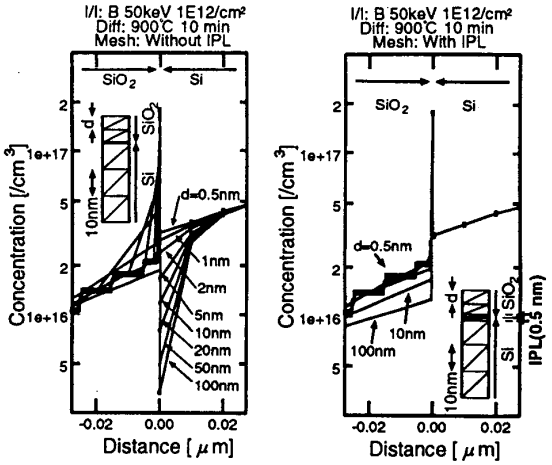
References

[1] S.Kumashiro and I.Yokota. *NUPAD V*, pp. 167–170, 1994.

[2] S.Ushio et al. *Solid-State Electronics*, Vol. 33, pp. 69–73, 1990.

[3] M.Kawata et al. *SSDM 95*, pp. 360–362, 1995.

[4] Richard B. Fair. *IEDM 95*, pp. 85–88, 1995.



(a): Conventional mesh. (b): Proposed mesh.

Fig.1: An interface concentration of the boron: The diffusion simulation on an oxide/silicon structure is examined. The case of the conventional mesh, the interface profile depends on the mesh sizes in the oxide. On the other hand, if the proposed mesh is used, the interface profile does not depend on the mesh sizes.

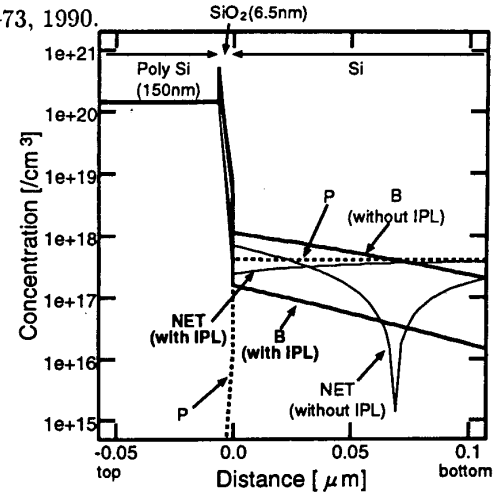


Fig.3: A comparison of diffusion profiles of the phosphorus, boron and net ($N_D - N_A$) with and without the IPL. The gate oxide thickness is 6.5nm and the gate electrode was prepared from undoped 150nm-thick polysilicon implanted with BF_2 at 50keV and a dose of $3\times10^{15}\text{cm}^{-2}$. Subsequent N_2 annealing was carried out at 1000 ℃ for 1 hour. In the case of no IPL, the edges directly connect the oxide/polysilicon interface to the silicon/oxide interface, so that the boron diffusion is enhanced significantly. This difference of the channel profile causes about 1 V threshold voltage shifts as shown in Fig.4.

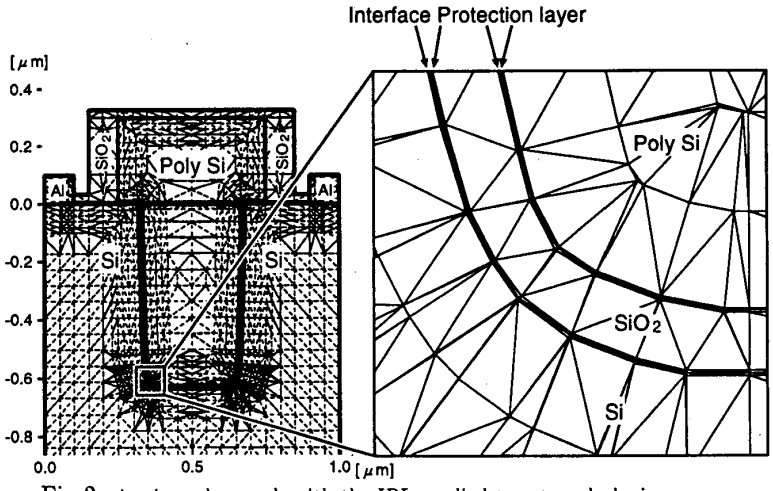


Fig.2: A triangular mesh with the IPL applied to a trench device.

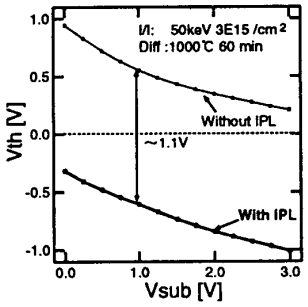


Fig.4: Vth vs. Vsub.

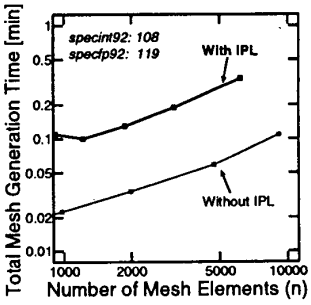


Fig.5: CPU-time for the mesh generation.