Advanced Geometric Techniques in 3D Process Simulation

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The modeling of semiconductor devices in the deep submicron era is a complicated and challenging procedure. Due to continuous scaling of IC structures many physical effects pose requirements for a full 3D simulation. The incorporation of advanced computational geometry techniques is imperative in the realization of such 3D process simulation tools. The simulation of a virtual factory, with the various processing steps (ion implantation, diffusion, oxidation, etching and deposition) directly modeled on a 3D tetrahedral grid presents many advantages, such as the direct geometry extraction for subsequent interconnect analysis and device simulation. Advanced geometric techniques for the realization of a virtual IC fabrication simulator directly on a 3D tetrahedral grid are presented. A highly efficient algorithm for refining unstructured tetrahedral meshes, having an O(n) computational complexity which generate very high quality elements, is used as the main tool for adaptive mesh generation [1,2]. Techniques for the automatic grid formation based on the mask layout and processing information and deposition of material layers are also presented.

Mesh Refinement

Mesh refinement is accomplished with the insertion of new nodes and the successive subdivision of the elements (Fig.1a). The insertion of new nodes on the finite element mesh has as a result the degradation of elements' quality. Mesh quality is improved by the application of Delaunay transformations on tetrahedra and the repositioning of nodes.

Tetrahedral Delaunay Transformations - Node Repositioning

A set of topological transformations are applied on the tetrahedra so that a high quality grid is generated. The topological transformations are based on the geometric theory of Voronoi-Delaunay. Two neighboring tetrahedra that have a face on a common interface can be transformed with the exchange of the common diagonal (Fig 1b). Two tetrahedra that have a face in common and do not satisfy the Delaunay empty sphere criterion can be transformed into three tetrahedra (Fig 1c). The inverse transformation is also possible, three tetrahedra with a common edge can be transformed into 2 tetrahedra by deleting their common edge.

Node repositioning is accomplished by the movement of a node towards the barycenter of the polyhedron formed by the surrounding tetrahedra. An analog case in 2D with a triangular mesh is shown in Fig. 1d. However the positioning of the node directly on the barycenter is very probable to result in overlaping tetrahedra, since the sorrounding polyhedron may be non-convex. In order to circumvent this difficulty a procedure is employed based on a variable projection movement. The procedure is complicated and extra connectivity structures are formed so that it is implemented efficiently (with O(n) computational complexity) [2].

The iterative application of the Delaunay Transformations and the node repositioning consist the optimization algorithm which has as a result the generation of high quality tetrahedral meshes with most of the elements having a nearly equilateral shape and totally avoiding the formation of sliver tetrahedra.

Mask Patterning on the Wafer Exposed Surface and Layer Deposition

The mask layout can be patterned directly on the exposed surface of the tetrahedral grid (Fig.2a). The steps for doing this are a) projection of the mask on the exposed surface, b) exposed surface face refinements on mask's segments junctions, c) refinement of surface edges that cross mask's segments. In all of these steps mesh conformity is preserved so that the boundaries between tetrahedra are preserved.

The Deposition of a new layer is accomplished by extruding the surface faces of the exposed surface and the generation of a layer of prisms, as is shown in Fig2b. Then the prisms are divided into tetrahedra so that conformity of the mesh is preserved.

Application - Modeling of a CMOS Structure

The above techniques have been incorporated into Aristotle, a Finite Element Analysis System written in C with a GUI based on X/Motif. Application to the modeling of a CMOS structure is presented in Fig. 3. The active regions are patterned on the mesh and the n-well region is modeled using heavy refinement (Fig 3a). A thin layer of oxide is deposited, and in the following oxidation and polysilicon gate deposition are modeled as is presented in Fig. 3b.

References

[1] N. A. Golias, Ph. D. Thesis, Aristotle University of Thessaloniki, Greece, 1993.
[1] N. A. Golias, T. D. Tsiboukis, Int. Journal for Numerical Methods in Engineering, **37** 793-812, 1994.

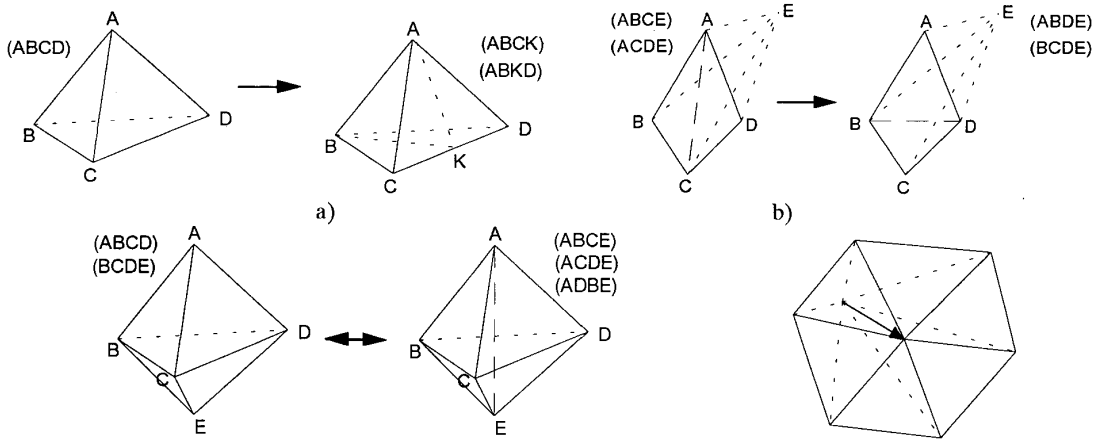
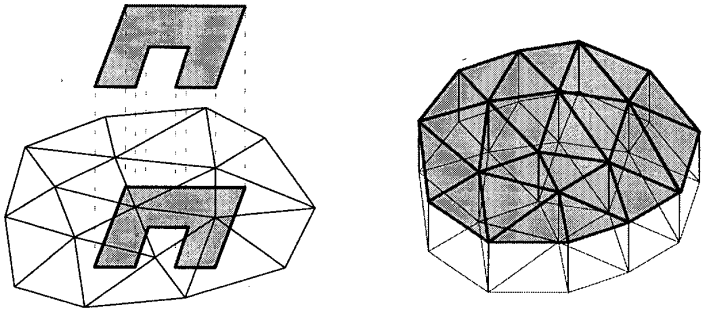
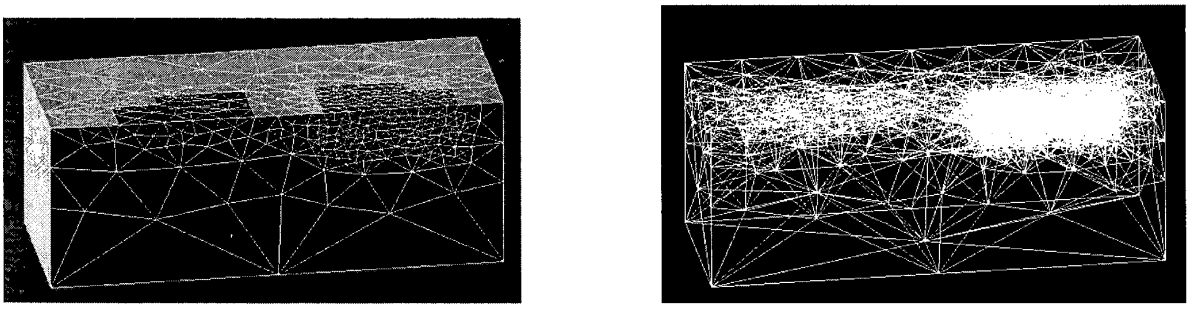


Fig. 1. Geometric Techniques for 3D Unstructured Tetrahedral Grids.

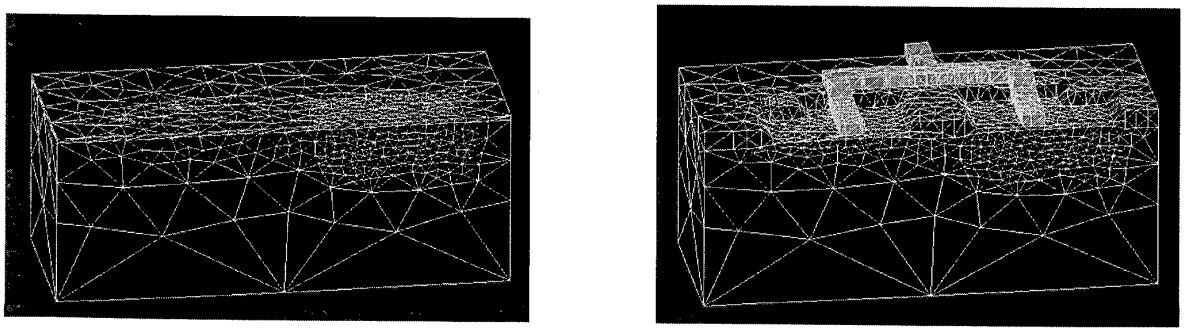


a) b)

Fig. 2. Mask Patterning and Tetrahedra Layer Deposition



a) Active regions patterning and heavy refinement in the n-well region.



b) Deposition of Oxide layer, Oxidation and Deposition of Polysilicon Gate

Fig. 3. Simulation of a CMOS structure