# Accurate Chip Scale Topography Modeling in O(n) Run Time

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## 1. Introduction

Currently, semiconductor manufacturing topography models for design and process optimization can investigate only a tiny portion of a die at a given time. Therefore, important coupling effects between areas are ignored. As interconnect capacitance and resistance become the limiting factor to chip speed, the coupling effects of process variations upon timing delays will become critical. Additionally, current process models are unable to consider known die scale effects such as stepper lens aberrations, tilt, scaling, polishing variations and etch loading effects. We are introducing a model for accurately simulating die scale effects upon semiconductor topography in O(n) run time, where n is the number of mask features, and with efficient memory usage. The inherently parallel model combines existing process models with new developments. The model provides a better interface between design and process areas for complete die performance optimization studies.

## 2. Previous Work and Extensions

Recent developments in process simulation have shown the potential to quickly and accurately predict the aerial image from large mask areas (e.g. [1][2]). Other work has linked this image to photoresist (resist) diffusion and approximate development models[3]. We have extended these methods by combining a parallel tiling algorithm for complete die aerial image calculation with common O(n) run time scalar lithography simulation techniques. We are also introducing a more accurate approximate development model which allows the addition of etch models. Efficient wafer feature storage allows the storage of near chip sized layouts on an engineering workstation with minimal loss in accuracy. Our method uses accurate physics models to account for the effects of photomask patterns, stepper characteristics and substrate thin film interference effects. The method uses the powerful combination of design tool extraction capabilities and tuned high precision process models to model the chemical effects of resist diffusion, resist development and etch loading as a function of feature size and local environment.

## 3. Model Description

The process flow for our model is given below.

- **1** *Calculate light intensity vs. vertical position in resist for all possible substrates and resist thicknesses. Fit results to a line to model resist diffusion. Store relative intensity at top, middle, bottom of resist. Assumes open frame exposure.*
- **2** *Calculate aerial image at top of resist for subset of mask. Only compute intensity at points near mask feature edges.*
- **3** *Compute resist diffusion horizontally by gaussian smoothing of intensities at points.*
- **4** *Use development approximation to compute resist feature edge points using intensity threshold given by tuned full simulator. Threshold value can be function of feature size, defocus, and location in resist (top, middle or bottom).*
- **5** *Reduce number of stored points in resist features along linear edges by checking which points are necessary.*
- **6** *Repeat steps 2-5 for middle and bottom of resist. Recompute defocused aerial image as it travels through resist.*
- **7** *Merge points along boundaries of subsets by taking average location.*
- **8** *If desired, approximate point movement based etch model can be applied.*
- **9** *If desired, resulting features can be read into design tools for processing or comparison to layout.*

The method uses decoupling of the horizontal and vertical effects of imaging and diffusion as in scalar lithography models. Light intensity is calculated only at points near mask feature edges to save run time and memory. The development approximation stores resist features as polygons similar to layout languages, reducing memory usage and allowing easy import back into design tools. Aerial image computed at three resist planes to incorporate surface, bulk and substrate resist effects. Resist feature size changes due to non-uniform substrates are approximated to first order by thin film effects. We used the rigorous non-planar lithography model Metropole[4] tuned to experimental results to ensure high accuracy resist profile results.

## 4. Results

Figure 1 shows the tiling algorithm including the overlaps necessary to ensure aerial image correctness. Figure 2 shows how

the resist features are extrapolated from the intensity grid. Figure 3 shows the aerial image of the Nikon test mask calculated using an FFT method in ~6 seconds on an HP 725 workstation. The subset size is non-optimal but the optimal dimensions can easily be determined from λ and the run time of the aerial image method (O[nlogn] for FFT). Doubling the subset size shown and assuming a $1mm^2$ area, the model gives a nonparallel run time of ~83 hours. Most of this time is spent in aerial image calculation where [2] has reported large speedups over the FFT method. The dense features in Figure 3 can be stored accurately using only ~500-1000 points each requiring 8 bytes for a total memory usage in 3 layers of ~12-24KB. Assuming a 60% lower feature density for a typical logic polysilicon gate layer, memory usage for a $100mm^2$ area would then be ~3.5-7GB. Figure 4 shows how the values for the threshold resist development model are obtained from the tuned rigorous simulator.

## References


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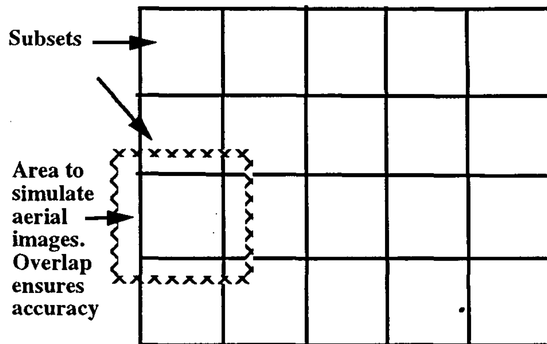



Figure 1. Tiling algorithm for decomposing large mask area into quickly simulated subsets. Simulation area is larger than subset by ~10λ per side to ensure correctness.

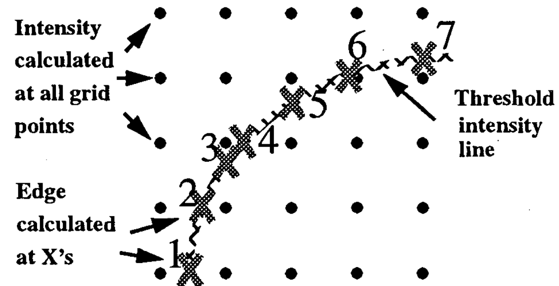



Figure 2. Computing edge points of feature from intensity grid. Intensity threshold used to compute edge location vertically and horizontally between points. Unnecessary points (e.g. #3 above) removed by determining if they lie on line between neighboring points within error criteria.

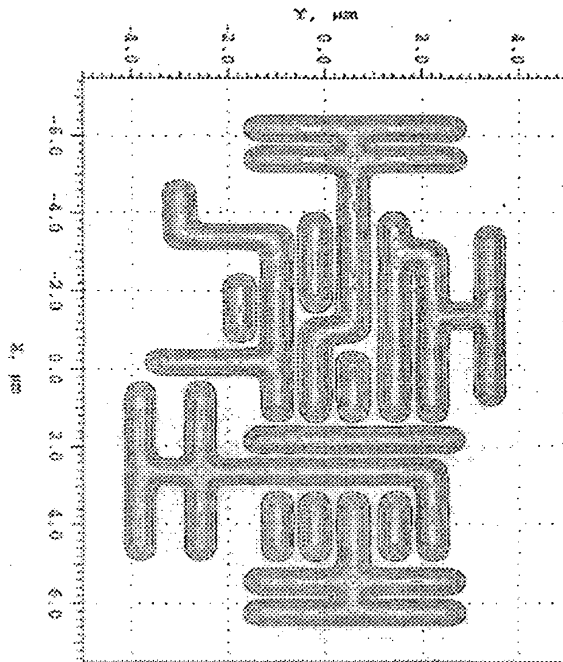
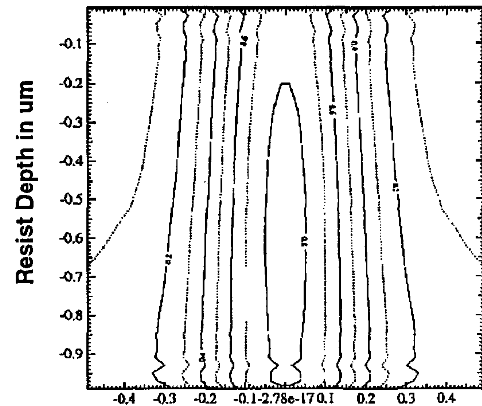


Figure 3. Aerial image of Nikon test mask computed in ~ 6 seconds using FFT method.



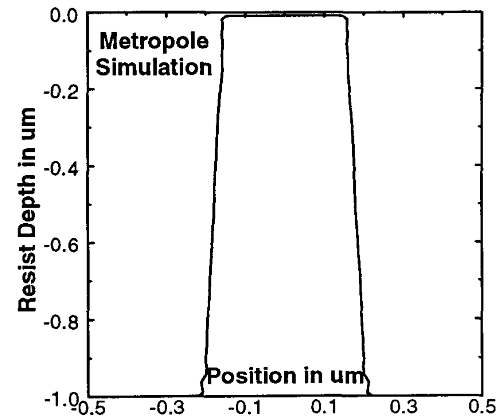




Figure 4. Internal light intensity and final resist profile from Metropole simulation. Threshold easily computed vs. depth.