6-5

TCAD Diagnosis of I/O-Pin Latchup in Scaled-DRAM

Katsumi Tsuneno, Hisako Sato, Seiji Narui, and Hiroo Masuda
Hitachi, Ltd., 2326 Imai, Ome-shi, Tokyo, Japan

Abstract

This paper describes a TCAD analysis of I/O-pin Latchup failure found in a shallow-well CMOS DRAM. The 0.35um DRAM I/O-pin showed significant degradation in latchup test of JEDEC Standard over-current stress. TCAD diagnosis of the failure was conducted and newly clarified its biasing effect of guard-band (N^+) layer and the layout-related latchup mechanism, which leads to an practical latchup-immunity design in sub-um CMOS process and layout. To overcome process-margin problem against latchup, a simple CMOS process is proposed for the 0.35um DRAM.

Experiment

A Mega-bit DRAM was fabricated with a 0.35 um CMOS with shallow well process [1]. The DRAM layout of an I/O buffer NMOS is shown in Fig. 1. As shown in the layout, a N+ guard band layer is formed to prevent possible minority carrier injection due to input-pulse undershoot[2] and ESD surge. Since the shallow-well structure enhance vertical current gain of NPN and PNP BJT's, latchup design is one of the key factors in the DRAM layout and process.

An anomalous degradation in latchup test was found in JEDEC Standard over-current stress test, as shown in Fig. 2. The figure shows optical emission measurement which identify the current path under the latchup condition. The maximum latchup trigger current (Imax: maximum allowable injection current from I/O-pin before latchup) was less than 10 mA including experimental variations. It is noted that the latchup failure was not observed in the identical test in conventional deep-well process (Imax>1A). The latchup current path was determined based on the optical-emission measurement (Fig. 2), which identified a parasitic SCR of peripheral $\underline{P}^+$(PMOS drain) $\underline{N}$ (shallow-well) $\underline{P}$ (substrate) and $\underline{N}^+$ (NMOS source) structure, located 100um apart from the I/O NMOS buffer devices as shown in Fig. 1.

Simulation Diagnosis

TCAD analysis was conducted to diagnose latchup in 2D for the whole sectional structure shown in Fig. 3. As shown in the figure, the N^+ guard-band in an N-well is formed. Simulated result of latchup current is shown in Fig. 4. The following five-step-trigger mechanism is characterized in this latchup phenomena.

(1) I/O N^+P junction breakdown mode.

(2) Lateral NPN turn-on between I/O and guard-band N^+ layers, which accumulates holes in the substrate.

(3) The hole accumulation triggers on the Lateral NPN between the peripheral N-well and NMOS N^+ layers.

(4) Build-up voltage drop in N-well due to (3).

(5) PNPN SCR operates in the peripheral CMOS, caused by forward biasing of P^+N-well diode.

As described above, N^+ guard-band plays an important role in the latchup triggering-steps, therefore, we studied the N^+ guard-band effect on the latchup trigger current (Imax). TCAD simulation results are shown in Fig. 5. It is found that the N^+ guard-band biased at 0V turns out to be most latchup-immune structure over the other conditions, by a factor of >30. This is because the grounded guard-band absorbs the injected current effectively as well as prevents the hole accumulation in the p-type substrate.

To improve process-margin against latchup, a simple new CMOS process is also proposed and verified its effectiveness based on TCAD analysis. Proposed process and device structure is shown in Fig. 6, which introduces a new buried P^+ layer (high energy implant, peak density = $6x10^{16}$ cm^{-3}) to reduce hole-current flow which turns on the NPN transistor in the SCR structure. Latchup analysis exhibits an excellent latchup immunity in the new process (Imax=6mA/um) over a conventional one (Imax=0.2mA/um).

TCAD analysis on I/O-pin junction-breakdown is verified with experimental I-V curve as shown in Fig. 7, showing good agreement within the BVds(min) error of less than 1V. The experimental latchup trigger-current (Imax=5-10mA) satisfies reasonable agreement with TCAD simulation results, by taking into account the effective width of 25-50um in latchup current path (see physical layout in Fig. 1). However, 3D analysis will be necessary in future quantitative latchup-design.

References

[1] H. Masuda et al.; "A 5V-only 64K Dynamic RAM Based on High S/N Design", IEEE J. of SSC Vol. sc-15, pp.846-854, October 1980.

[2] H. Masuda et al.; "TCAD Strategy for Predictive VLSI Memory Development", IEDM'94 Tech. Paper, pp.153-156, December 1994.

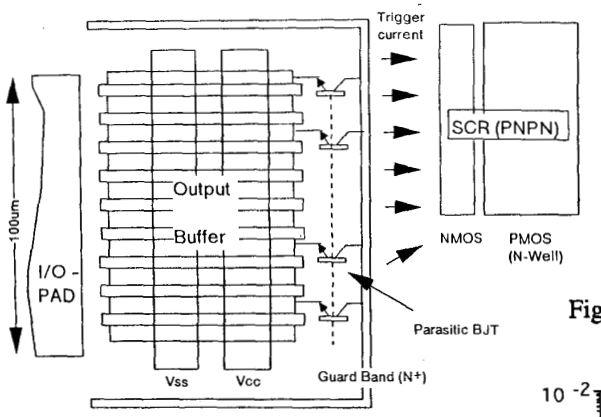

Fig. 1 Layout of a DRAM I/O buffer.

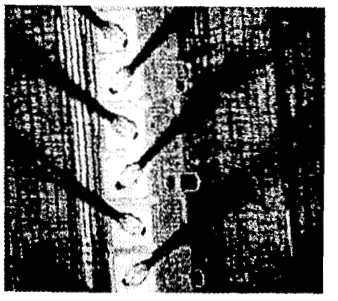

Fig. 2 Optical emission measurement of current path under the latchup.

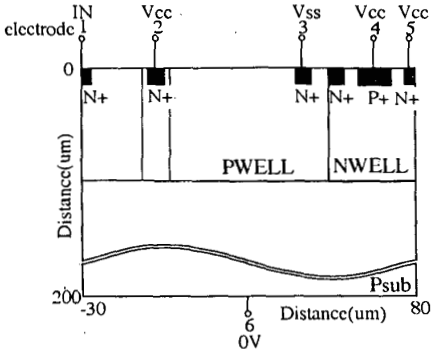

Fig. 3 Sectional structure for TCAD diagnosis.

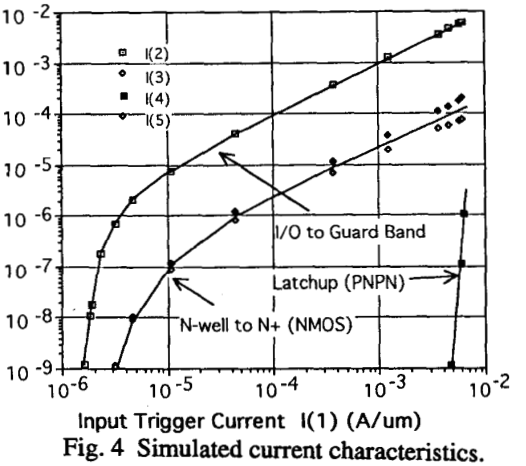

Fig. 4 Simulated current characteristics.

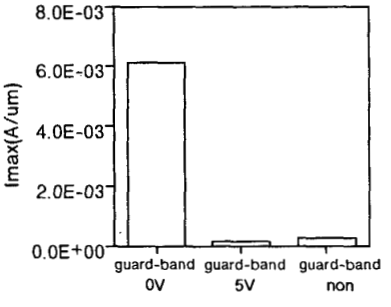

Fig. 5 N^+ guard-band effect on the latchup trigger-current (Imax)

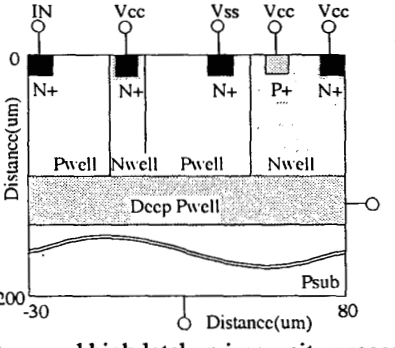

Fig. 6 Proposed high latchup immunity process with high-energy implant buried P+ layer.

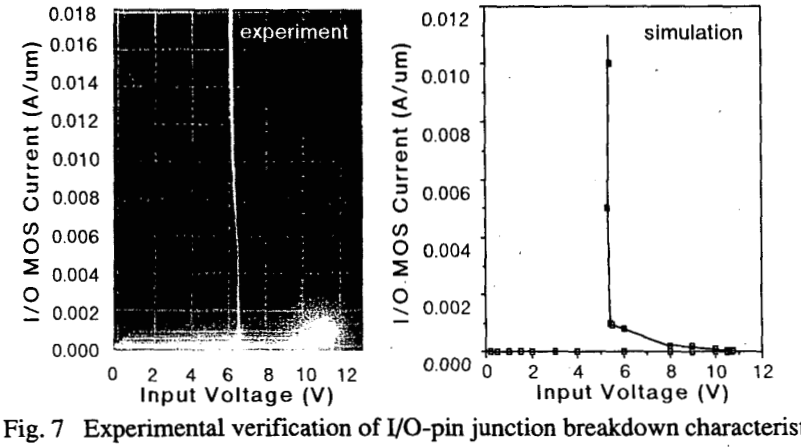

Fig. 7 Experimental verification of I/O-pin junction breakdown characteristics