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An Integrated TCAD System for VLSI Reliability Simulation

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I. Introduction

The reliability problems, such as ElectroStatic Discharge(ESD) and latch-up, are very important issues in VLSI circuit design. However, performance evaluation using a trial-and-error method on real Test Element Group(TEG) manufacturing and measurement requires impractical turn-around time and expense. Moreover, the analysis about internal characteristics based on physics cannot be obtained using the conventional method. To overcome these problems, TCAD simulations have been widely used to solve the various reliability problems. However, since most circuit designers, who are in charge of layout strongly related to the reliability problems, are not familiar with complicate TCAD tools, the need of a more effective and convenient simulation environment has been increasing.

II. System Requirements of SANTA

SANTA(SAmsung's Navigator for TCAD Applications) is an integrated TCAD system which provides a simulation environment for reliability analysis and VLSI technology development. It consists of several tools controlled by Simulation Manager, as shown in Figure 1. Structure Editor is a front-end tool to generate grids and mask geometries for process simulation through the graphical user interface. The generated data and the calibrated TCAD simulation libraries are used to make a process/device simulation flow. Figure 2 shows the splitted simulation flows with some tools. After making a simulation flow, users can apply Response Surface Method(RSM) using pdExperiment, pdWorksheet and pdDiagnosis[1] to design the process/device control variables and to optimize those values. The designed simulation inputs are loaded on the assigned computers for process/device simulation via the queuing and distribution system called Job Load Balancing System(JLBS). Then, SPICE MOSFET model parameters can be extracted by Advanced MOSFET model Parameter EXtractor(APEX)[2] from simulation results.

To build an useful environment for reliability simulation, firstly, many kinds of calibrated simulation libraries are needed. Figure 3 describes TCAD Simulation Library which enables users to reduce the time to generate simulation input files and provides the simple simulation method with expert knowhows. *FabRecipe* includes the calibrated input files corresponding to the fabrication recipes of unit processes. *Process* and *Device* provide a variety of process and device simulation examples. *Reliability* includes libraries regarding reliability simulation like ESD and latchup. In the case of ESD simulation, various equivalent models for ESD pulses and protection circuits are provided. These libraries are constructed by the modeling for various equipments and protection schemes. Secondly, library management tools, such as schematic capture, layout editor and browser, are needed. Finally, the functions of tool calibration, optimization and visualization specific to reliability performance must be supported.

III. Application Example

The input and address stages of a MASKROM device are designed as a form of finger transistors to protect a ESD pulse by using parasitic bipolar effects[3]. We have used a mask for plug implantation to prevent the high current localization of the finger transistors[4]. The purpose of this application is to determine an appropriate size of the transistor without the plug implantation step. The equivalent model of the ESD pulse on the input stage, Human Body Model 3000(V), and a protection(finger) transistor are shown in Figure 2. The experimental variables are the length, width of finger transistor in both cases of with and without the plug implantation. Simulation input files are generated by full factorial method(total 24 cases).

Simulation results displayed by SANTA show that the major cause of ESD failures is local temperature overheating in the drain to the substrate junction area(Figure 4). As shown in Figure 5, it can be seen that the maximum lattice temperature can be controlled by the length and width of the finger transistor such that using the wider width or the shorter length produces the lower maximum temperature. In Figure 6, the maximum temperature of the previous plug-implanted MASKROM device with W/L=300μm/2.0μm is 510° K. Since through the real manufacture and measurement, the device was proved its reliability against the HBM 3000(V), we can assume that devices whose maximum temperature values don't exceed line ① have the same ESD immunity. Thus, when the device manufactured without plug implantation has its width of equal or larger than 400um, it acts the same ESD protection as the device with plug implantation. As a result, well selected device size (W/L=400μm/1.0μm) optimized on SANTA can eliminate an additional process step while maintaining the same ESD performance. After the manufacturing again, the new device can pass the same ESD test.

IV. Conclusions

SANTA is a useful environment to both VLSI technology developer and circuit designers who are not familiar with complex TCAD tools. Through the ESD protection application, we find that a well selected device width and length can reduce process steps without loosing performance threshold.

References

[1] Pdfab User's Manual, PDF Solutions, 1994.

[2] Chang-Hoon Choi, Jin-Kyu Park, Yeong-Gil Kim, Kyung-Ho Kim, and Sang-Hoon Lee, "New Model Parameter Extraction Environment for the Submicron Circuit Models", ISCAS, p.1535-1538, 1993

[3] Neal K. Clark, Krishna Parat, Timothy J. Maloney, and Yudong Kim, "Melt Filaments in n^+pn^+ Lateral Bipolar ESD Protection Devices", EOS/ESD Symposium Proceedings, p.295-303, 1995

[4] Sabbas Daniel and Gadi Krieger, "Process and Design Optimization for Advanced CMOS I/O ESD Protection Devices", EOS/ESD Symposium Proceedings, p.206-213, 1990

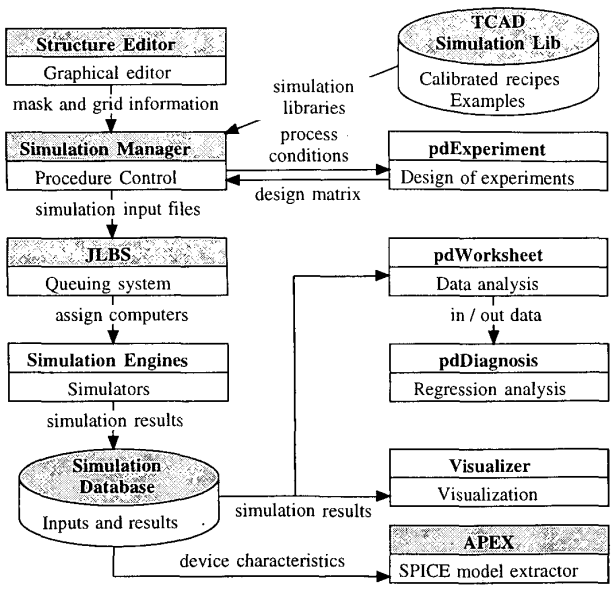

Figure 1: SANTA system and its data flow.
□ : Internal tools or database, ■ : External tools

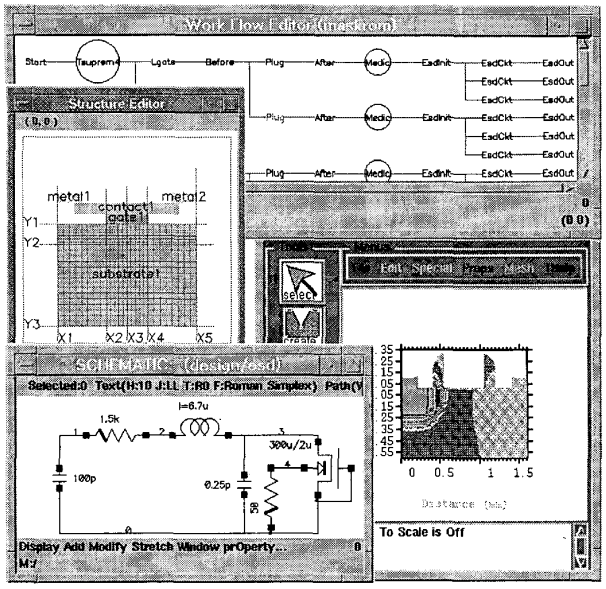

Figure 2: The splitted simulation flows and some tools.

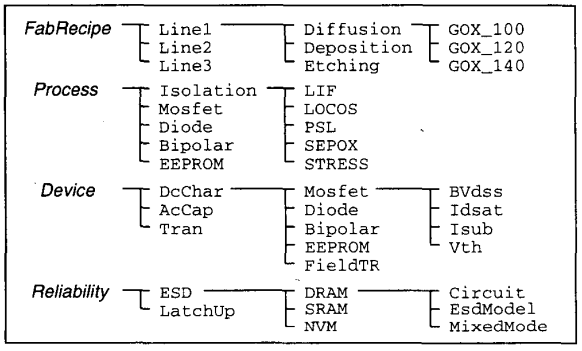

Figure 3: The tree example of TCAD Simulation Library.

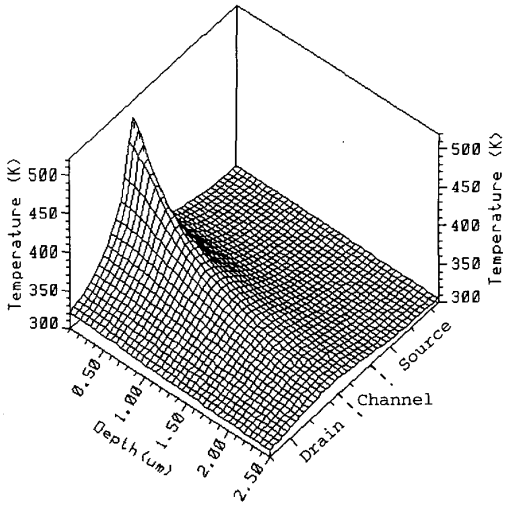

Figure 4: The Distribution of lattice temperatures.

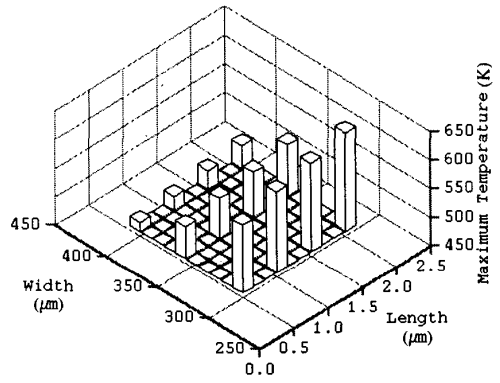

Figure 5: Maximum lattice temperatures vs. width and length of the finger transistor without plug implantation.

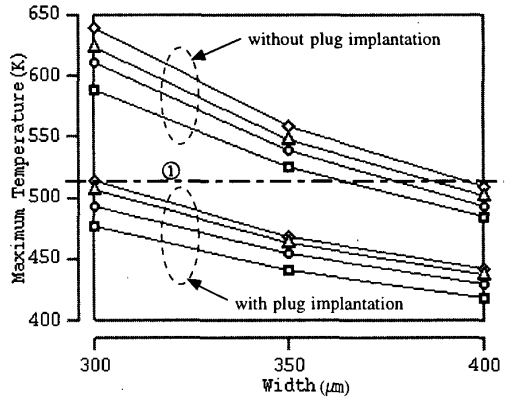

Figure 6: Maximum lattice temperatures of 24 cases.
Length(□ : 0.5, ○ : 1.0, △ : 1.5, ◇ : 2.0μm)