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Two-Dimensional Simulation of Surface-State Effects on Slow Current Transients in GaAs MESFETs

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GaAs MESFETs are essentially high-speed and high-frequency devices. However, slow current transients were often observed experimentally even if the drain voltage or the gate voltage changed abruptly. They were called "drain-lag" or "gate-lag" and could be fatal when high-speed operation was considered, but the mechanisms were not clear. Recent studies by 2-D simulation indicated that the drain-lag could occur due to deep levels in the semi-insulating substrate [1],[2]. As for the gate-lag, effects of surface states were suggested, but the detailed mechanism was not well clarified. In a previous work [3], we made primary simulations of GaAs MESFETs including surface states and found that the gate-lag could arise depending on the nature of surface states. So, in this work, we have made more systematic simulations and studied how the gate-step-responses are affected by surface-state's energy level, surface-state's density, and deep levels in the substrate. As a result, we have obtained a clearer knowledge on why the gate-lag arises and how it can be reduced.

Fig.1 shows device structure simulated here. The gate length is typically 0.3μm. For the surface state model, we adopt the Spicer's unified defect model [4]. We assume that the surface states consist of a pair of deep donor and deep acceptor and the following two cases based on experiments are mainly considered for GaAs surface [4],[5].

a) Sample 1: $E_{SD} = 0.925$ eV, $E_{SA} = 0.8$ eV, b) Sample 2: $E_{SD} = 0.87$ eV, $E_{SA} = 0.7$ eV.

where E_{SD} is energy difference between the bottom of conduction band and deep donor's energy level, and E_{SA} is energy difference between deep acceptor's energy level and the top of valence band. The surface states are assumed to distribute uniformly within 5 Å from the surface. Their density and capture cross-section for carriers are typically set to 10^{13} cm^{-2} (2×10^{20} cm^{-3}) and 10^{-15} cm^2, respectively. For a substrate, we consider undoped semi-insulating LEC GaAs where deep donors "EL2" compensate shallow acceptors [2]. Basic equations are Poisson's equation, continuity equations for electrons and holes, and three rate equations for the deep levels. These are solved numerically in two dimensions.

Here we calculate turn-on characteristics of GaAs MESFETs when the gate voltage changes abruptly. The previous work [3] suggested that the deep-acceptor-like surface state mainly determined the Fermi-level position at the surface. So, to clarify the roles of deep-acceptor-like state, we consider here a case with the deep acceptor only. Fig.2 shows the calculated turn-on characteristics as a parameter of E_{SA}. The curves for $E_{SA} = 0.8$ eV and 0.7 eV are essentially consistent with those for Sample 1 and Sample 2, respectively, where the deep-donor-like state is also included. So, we can say that the turn-on characteristics are determined by the deep acceptor and that slow current transisnts are more remarkable when the deep acceptor locates nearer to the valence band. Fig.3 shows comparison of potential profiles for the OFF states, and Fig.4 shows profiles of the ionized deep-acceptor density N_{SA}^- along the surface. It is seen that for $E_{SA} = 0.8$ eV, the channel is essentially shut down under the gate and N_{SA}^- changes little between OFF and ON states. But, for $N_{SA} = 0.7$ eV, the channel is entirely depleted from source to drain and N_{SA}^- changes much between OFF and ON states, so the slow current transient due to the deep acceptor arises in this case. This difference in potential profiles is originated from the fact that the deep acceptor acts as an "electron trap" for $E_{SA} = 0.8$ eV and it acts as a "hole trap" for $E_{SA} = 0.7$ eV.

To reduce the slow current transients, the deep acceptor should be made electron-trap-like. This can be realized by reducing the surface-state density, as described below. Fig.5 shows calculated turn-on characteristics for Sample 2 ($E_{SA} = 0.7$ eV) with different surface state density N_S. At low N_S of 2×10^{19} cm^{-3}, the slow transient is not observed. Note that in this case, the potential profiles show an electron-trap-type feature, as seen in Fig.6(a). Fig.7 shows Fermi-level position at the surface versus N_S at zero bias for Sample 2. In this figure, E_{SA}^* is a level called "the equality level" in the SRH statistics, and if the Fermi level lies above (under) it, the deep acceptor acts as electron trap (hole trap). From this, we see that by reducing the surface-state density and raising the Fermi level at the surface, the deep acceptor can be made electron-trap-like.

Finally, we briefly describe effects of deep levels in the substrate on turn-on characteristics. Fig.8 shows calculated turn-on characteristics for a case with semi-insulating substrate. Its effect is observed particularly in Sample 1 as a slight increase in drain current during $t = 10^{-2}$ to 10^0 sec. This increase occurs due to electron emission from deep donors "EL2" in the substrate, but its effect is not so large.

In conclusion, we have clarified the role of deep-acceptor-like surface state in slow current transients in GaAs MESFETs. To reduce them, the deep acceptor should be made electron-trap-like. This can be realized by reducing the surface state density.

[1] S.H.Lo and C.P.Lee, *Solid-State Electron.*, vol.34, pp.397-401, 1991
[2] K.Horio and Y.Fuseya, *IEEE Trans. Electron Devices*, vol.41, pp.1340-1346, 1994.
[3] K.Horio, K.Satoh and T.Yamada, *Proceedings of SISDEP/SISPAD'95*, pp.78-81, 1995.
[4] W.E.Spicer *et al.*, *J. Vac. Sci. Technol.*, vol.16, pp.1422-1433, 1979.
[5] H.H.Wieder, *Surface Sci.*, vol.132, pp.390-405, 1983.

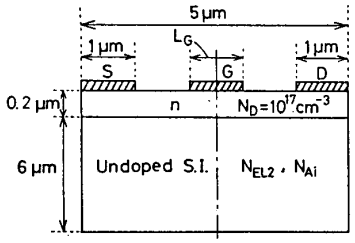

Fig.1 Device structure simulated in this study.

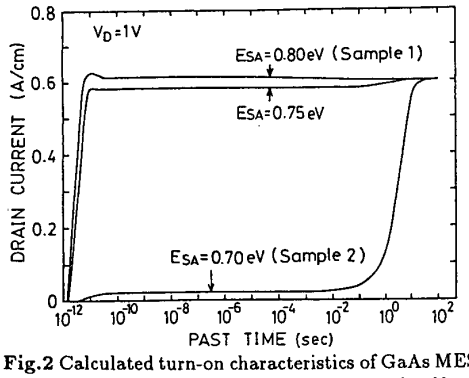

Fig.2 Calculated turn-on characteristics of GaAs MESFETs with deep-acceptor-like surface state only. $N_S = 2 \times 10^{20}$ cm^{-3}. Insulating substrate is assumed.

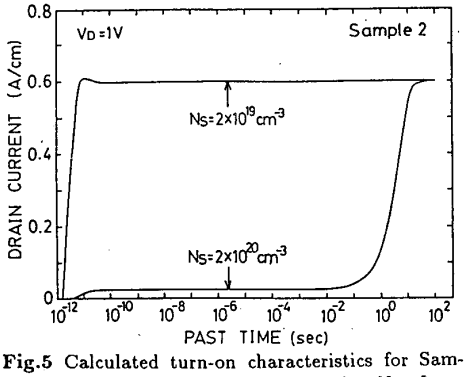

Fig.5 Calculated turn-on characteristics for Sample 2 with different surface-state density N_S. Insulating substrate is assumed.

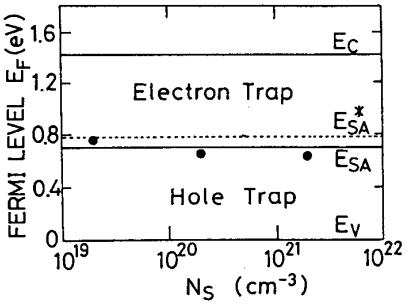

Fig.7 Fermi-level position at surface (●) versus N_S at zero bias for the case of Sample 2. E^*_{SA} is the equality level of deep acceptor.

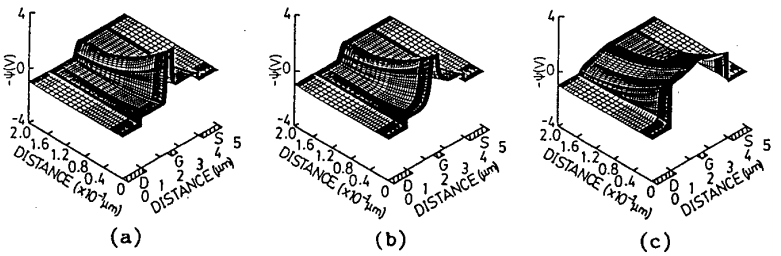

Fig.3 Comparison of potential profiles at OFF state with different E_{SA}, corresponding to cases in Fig.2. (a) $E_{SA} = 0.8$ eV, (b) $E_{SA} = 0.75$ eV, (c) $E_{SA} = 0.7$ eV.

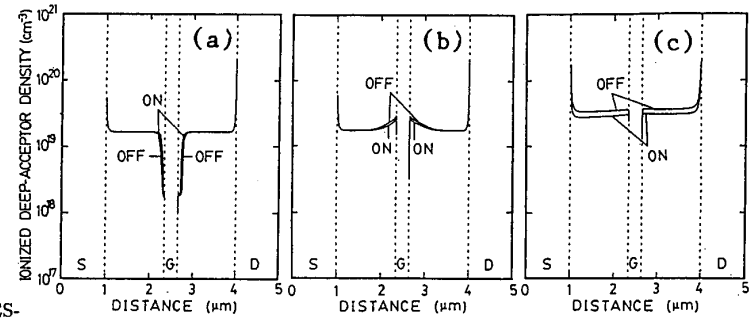

Fig.4 Comparison of ionized deep-acceptor density N^-_{SA} along the surface, corresponding to cases in Fig.2. (a) $E_{SA} = 0.8$ eV, (b) $E_{SA} = 0.75$ eV, (c) $E_{SA} = 0.7$ eV.

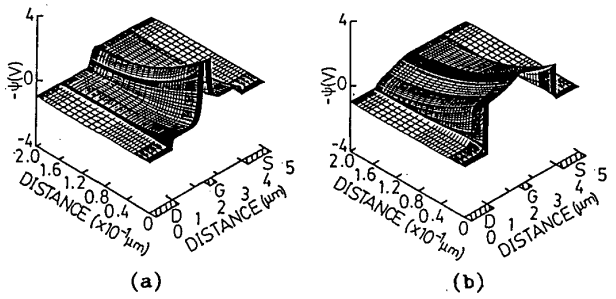

Fig.6 Comparison of potential profiles at OFF state with different N_S, corresponding to cases in Fig.5. (a) $N_S = 2 \times 10^{19}$ cm^{-3}, (b) $N_S = 2 \times 10^{20}$ cm^{-3}.

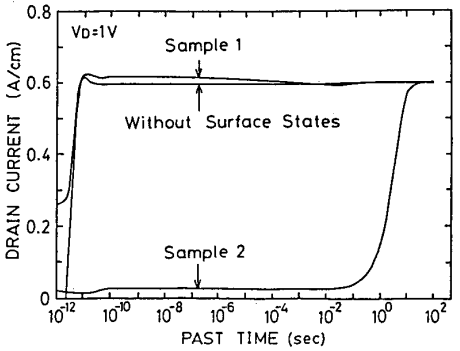

Fig.8 Calculated turn-on characteristics of GaAs MESFETs with semi-insulating substrate in which $N_{Ai} = 10^{16}$ cm^{-3} and $N_{EL2} = 10^{17}$ cm^{-3}. $N_S = 2 \times 10^{20}$ cm^{-3}.