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Numerical Simulation of Drain Lag in HJFETs with a p-Buffer Layer

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We studied the shielding effect of a partially depleted p-type buffer layer against traps for heterojunction FETs (HJFET). We confirmed a trade-off between the shielding and the drain parasitic capacitance. We also found a new frequency dispersion, which occurs in early stages due to the hole distribution setup time in the p-layer.

Drain lag caused by deep traps in the epi/substrate interface or in the substrate is a serious problem that interferes with using HJFET for wide-band applications such as digital ICs and MMICs [1]. Introducing a p-type layer under the channel, as is done with MESFETs, has been considered for shielding of traps. However, since selective doping is difficult for the epitaxially grown structure of HJFETs, the p-type layer must be carefully designed to shield the traps by undepleted holes, and to lower the drain capacitance by depleting the holes over a certain drain bias voltage.

To do this, we use a two-dimensional device simulator BIUNAP-CT, which incorporates Shockley-Read-Hall statistics for traps. Drain-p-layer capacitance is estimated by integrating the current from the p-layer. Step bias application to the drain confirms a trade-off between the shielding effect for traps and the drain capacitance. Also, a new drain current variation occurs at earlier stages. The variation is due to the time-lag in the formation of the steady-state hole concentration profile in the p-layer. Because of the difference in the channel length between the n-type intrinsic channel (0.3 μm) and p-layer length (7 μm), and the large difference in the drift mobility for electrons and holes, the time lag is about 10 times larger than the intrinsic speed of the FET. This can be another cause of problems for HJFETs. A detailed analysis is made of the new drain-lag and how to suppress it.

[1] K. Kunihiro and Y. Ohno: *GaAs IC Symposium Tech. Dig.*, pp. 267-270, 1994

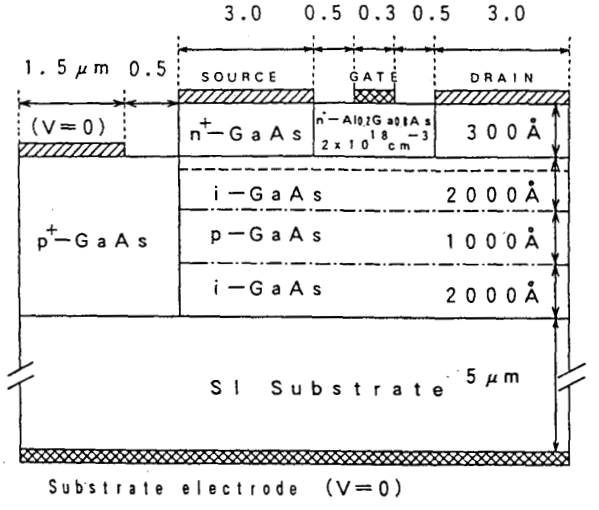

Figure 1: The device structure of a simulated AlGaAs/GaAs HJFET. The channel length is 0.3 μm. A p-layer is placed 2000 Å below the channel, with a thickness of 1000 Å. The concentration is varied from 1×10^{16} cm^{-3} to 2×10^{17} cm^{-3}. The p-layer is connected to the ohmic electrode.

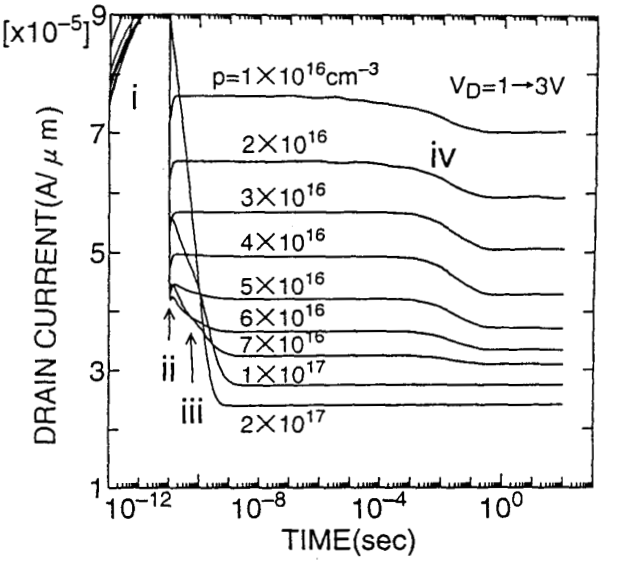

Figure 2: The transient response of drain current. The drain voltage is changed for a duration of 10 ps from 1 V to 3 V. (i) is the displacement current due to the bias change. (ii) is the setting up of the electron channel, which corresponds to the cut-off frequency of the FET. (iii) is the hole movement for the rearrangement of the hole distribution for the new drain bias. (iv) is due to the change in the trap charges.

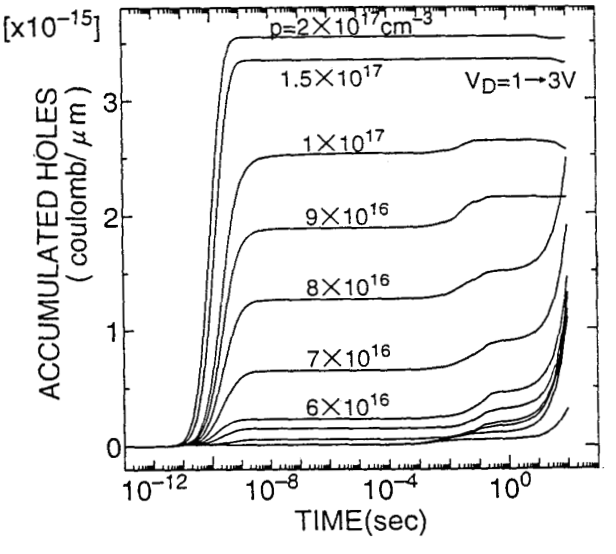

Figure 3: Integrated p-layer electrode current δQ, which is related to the effective drain-p-layer capacitance C_{eff} as, $\delta Q = \int I_p dt = \int_1^{V_p} C dV = C_{eff} \delta V_D = 2C_{eff}$, where I_p is the electrode current and V_p is the pinch-off voltage of the p-layer.

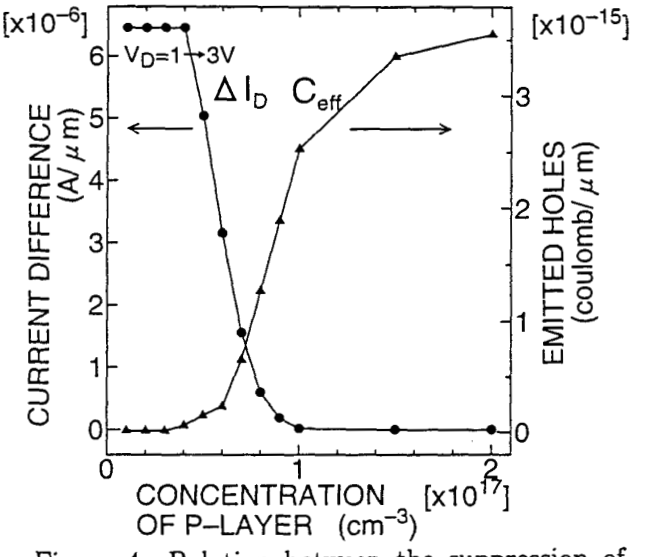

Figure 4: Relation between the suppression of drain current variation around 10^{-2} sec (which may be caused by the deep traps in the substrate) and the parasitic capacitance defined in Figure 3.