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Numerical Simulations of Surface States Effects on GaAs Power MESFETs

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The effects of surface states on the gate offset regions of GaAs power MESFETs are analyzed using a two-dimensional device simulator with a Shockley-Read-Hall statistics model for the surface states. Assuming electron trap type surface states (ET) and hole trap type surface states (HT)†, it is found that the trap properties cause a large difference in DC performance and pulse operation of the FETs.

An ungated drain region is indispensable in achieving a high drain breakdown voltage while maintaining high drain saturation current. However, it often causes a problem of slow drain current variation due to unavoidable surface states on the compound semiconductor surface. We performed farther extensive analyses beyond our preliminary simulation results[1] to investigate the detailed mechanisms and background physics.

At low drain and gate voltages, electric field strength along the channel is maximized at the gate electrode edge for the ET case, while it is maximized at the source/drain electrode edge for the HT case. This can be explained by the n-like or p-like behaviors of semiconductors with ET and HT, respectively, in the p(gate)-i(ungated region)-n(drain) structure of the surface. At higher biases, the peak electric field strength increases less for HT cases than ET cases because of trap charge saturation. For step bias application to the gate or drain, FETs with surface states show slow drain current transients after fast temporal drain current setups. The direction of the variations is opposite for ET and HT cases. This difference is explained by the trap charge variation during the period in which the potential distribution along the channel changes from temporal to final. The mechanisms that determine the time constants of the slow transients, together with the effect of the gate electrode material, are also investigated.

These results indicate that surface state control is essential in maintaining the proper surface electric field strength. They also show that the surface states can be evaluated by measuring the transient responses of the FETs. Therefore, these simulations will be indispensable for designing high-performance and stable-operation GaAs power FETs.

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[1] H. Nishizawa, H. Yano, N. Goto, and Y. Ohno, Tech. Report of IEICE, ED91-141, pp. 25-30(in Japanese), 1992

† ET and HT are defined as $Q_{TRAP} = f(n)$ and $Q_{TRAP} = f(p)$, respectively. The difference comes from the energy level (E_T) and capture cross sections (σ_n, σ_p) for the traps.

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Table 1. Simulated trap parameter.

Category	$\sigma_n(cm^2)$	$\sigma_p(cm^2)$	E_T-E_V(eV)	$N_T(cm^{-2})$	Label
Deep Acceptor	$1x10^{-14}$	$1x10^{-14}$	0.538	$2x10^{12}$	HT
	$1x10^{-14}$	$1x10^{-14}$	0.938	$2x10^{12}$	ET
Shallow donor	-	-	-	$1x10^{12}$	for HT and ET

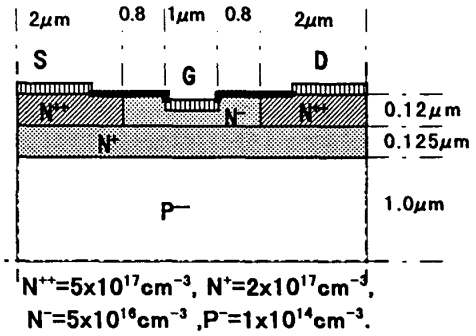
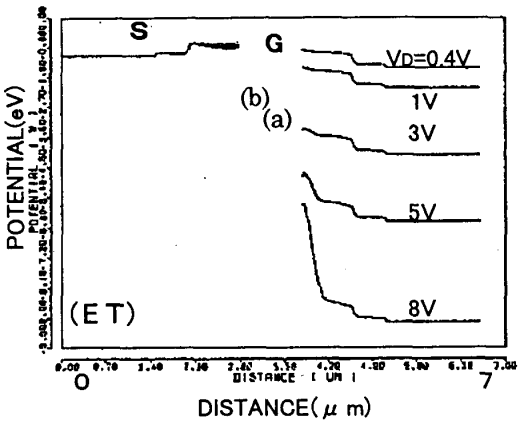


Fig.1 Simulated Device structure.
Surface states are assumed on the thick black lines. The states include two levels, a deep acceptor and a shallow donor of the half concentration of the deep acceptor, so that the total surface charge can vary from negative to positive.



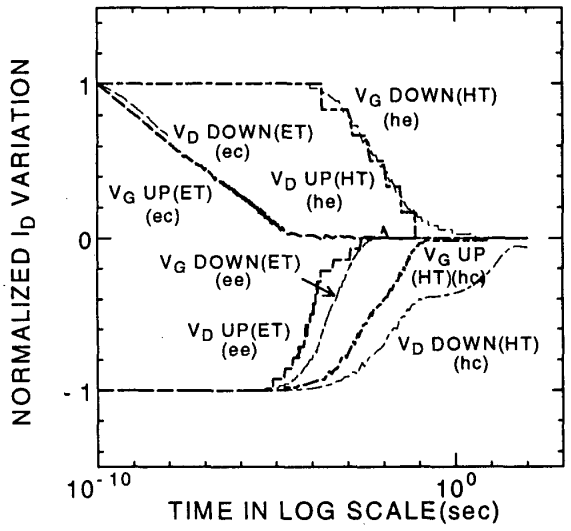


Fig.3 Normalized drain current variations. (ee), (ec), (he) and (hc) are electron emission, electron capture, hole emission and hole capture, respectively, for the main charge variation processes.

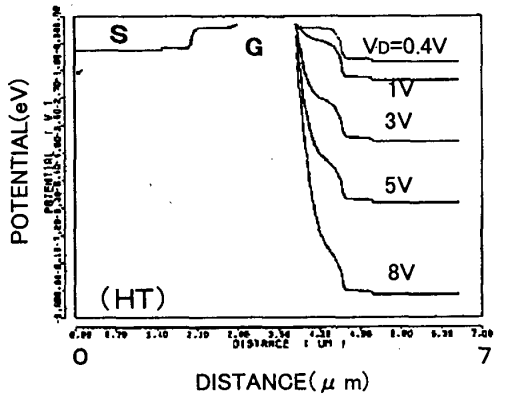


Fig.2 Potential profiles along the surface for various Vd's.
(a) ET, (b) HT.