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A Numerical Model for Simulating MOSFET Gate Current Degradation by Considering the Interface State Generation

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Abstract- In this paper, a new gate current degradation model for n-MOSFET's by considering the interface state generation is proposed. This interface state has been characterized using a new approach and been incorporated into a 2D device simulation for predicting the device gate current characteristics due to a hot carrier stress induced effect. Good agreements of the gate current have been achieved as compared with the measurement data for both fresh and stressed devices. This model is not only useful for predicting the gate current degradation, but also as a superior monitor than substrate current for submicron device reliability issues, in particular EPROM or flash EPROM devices.

1. Introduction

Channel hot-electron injection (CHEI) induced device degradation has shown a potential threat to the long term reliability of short channel devices [1]. Alternatively, the CHEI has also been widely used as the programming mechanism in EPROM or flash EPROM devices [2,3]. Therefore the model of the CHEI effect in MOSFET's is quite important for the understanding and design of future nonvolatile memory devices. In the past, either numerical or experimental technique has been employed to study the gate current [4,5], however, these models mentioned are only suitable for simulating the gate current of devices without considering oxide damages.

In this paper, we will first develop a new numerical simulation model of the gate current degradation by considering the stress induced interface state generation. The non-local effect for calculating the energy balance equation is also incorporated in this work [6]. Not only the gate current degradation in conventional MOS devices but also its applications and influence on EPROM device performance will be demonstrated.

2. The Gate Current Degradation Model

A set of equations, which comprises the Poisson equation, continuity equation, and an energy balance equation, along with a new gate current model is used to calculate the gate current degradation of n-MOS devices. Table 1 shows these equations and the model. Fig. 1 illustrates the flowchart for simulating the gate current in this work. Here, the energy balance equation [11] which takes the 2-D effect into account is given in Eq. (3), where, w_n represents the electron energy. τ_e and v_s are the energy relaxation time and electron drift velocity, respectively. Parameter κ is a fitting parameter and shows the 2-D transversal electric field effect. The gate current degradation characteristics due to the interface state generation is described in Eq. (4). In this study, we suggest that the interface state will cause the surface scattering and reduce the hot electron injection into the gate. As is shown in Fig.2, the measured gate current of a device after long term stress. It shows that I_G decreases with increasing stress time. Also, the total N_{it} can be calculated from Eq.(6) using measured values of the drain current. Eq.(5) is then used to calculate the spatial distribution of the N_{it}. Since I_G varies exponentially with N_{it} as in Fig. 3, the gate current of a stressed device can be described as the form in Eq.(4). Fig.4 gives the extracted spatial disrtibution of N_{it} for different stress time.

3. Results and Discussion

Floating gate measurement technique is used to measure the device gate current. Fig. 5 shows the gate current characteristics before and after the stress. The comparison of the gate currents among measurement data, our model, and previous work [6] without considering the surface scattering are also shown. The increase of gate current with stress time from previous model [6] is not correct by comparing with that measurement data since the surface scattering effect, and hence, the induced interface state was neglected. On the contrary, our model shows a decrease of the gate current with stress time, which is consistent with the measured data in Fig. 2. Also, from the comparison, our new modeled results are in good agreement with experimental results. Fig. 6 illustrates the calculated injection probability for fresh and stressed devices. The reduction of hot electron injection probability due to interface state generation is observed. The effective injection area is gradually shrunk with the increase of the interface state as we expected.

Since the channel hot electron injection is one of the general method to program EPROM or Flash EPROM devices, the reduction of gate current caused by programming operation will seriously affect the cell performance [7]. For a practical application, in Fig. 7, the transient characteristics of EPROM cell are simulated for devices before and after the stress. Serious retardation of programming time is observed due to a decrease of the gate current. This has been considered to be rather important for designing EPROM or flash EPROM after P/E cycles or long term operations. Therefore, degradation model of gate current caused by the oxide damages has played a dominant role in reliability issues for simulating device performance such as nonvolatile memory devices.

4. Conclusion

In this paper, a new gate current degradation model caused by the channel hot-electron stress induced interface state is developed. The simulation results calculated by this model is in good agreements with the measured data in n-MOSFET's. The effect of interface state generation on EPROM devices in terms of programming speed has also been studied and is believed to be the dominant

mechanism in device degradations. This is different from that reprted in previous work [6].

Owing to the importance of the generated interface state and the impact on device performance, the developed model is very useful for investigating the hot carrier reliability issues and for the design in EPROM and flash EPROM devices.

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References

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$$\nabla\varepsilon\nabla\Psi = -\rho \tag{1}$$

$$\nabla\cdot\vec{J}_n = -q\,(G-R) \tag{2}$$

$$\frac{\vec{J}_n\cdot\nabla w_n}{|\vec{J}_n|} + \frac{3}{5}\frac{1}{\tau_e v_s}(w_n - w_L) = \frac{3}{5}\frac{J_{nx}E_x + \kappa J_{ny}E_y}{|\vec{J}_n|} \tag{3}$$

$$J_G = -q\int_{w_B}^{\infty} n(x)v_z f(w,x)g(w)\exp(-\alpha_{ni}N_{it}(x))dw \tag{4}$$

where

$$N_{it}(x) = \overline{N_{it}}\int_{w_B} qn(x)v_z f(x,w)dw \Big/ \int qn(x)v_z f(x,w)dwdx \tag{5}$$

$$\overline{N_{it}} = \frac{1}{\alpha}\frac{\Delta I_D}{I_D}L_{eff} \tag{6}$$

Table 1 Set of equations and models for simulation of gate current characteristics.

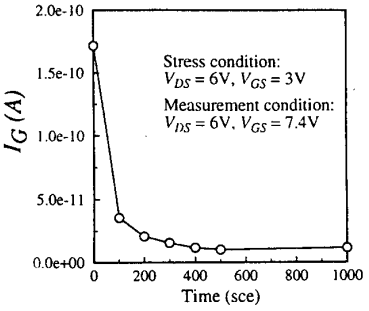

Fig. 2 The measured gate current variation with stress time.

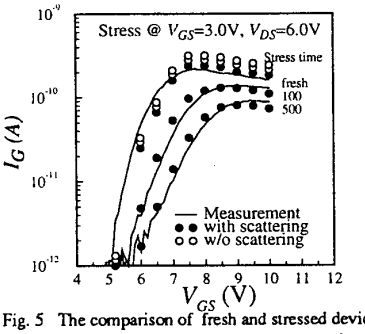

Fig. 5 The comparison of fresh and stressed device gate currents among the measurement data, our new model with mobility scattering, and without mobility scattering [6].

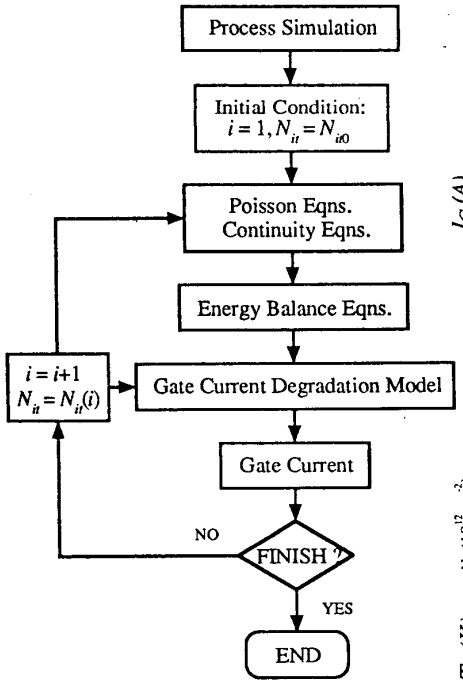

Fig. 1 Flowchart for simulating the gate current and device degradations.

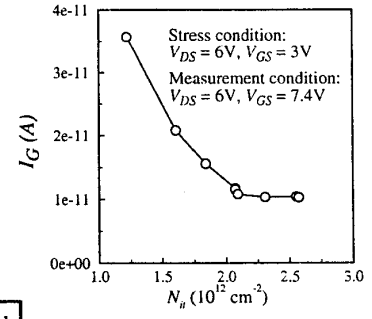

Fig. 3 Correlation between measured gate current and the interface states.

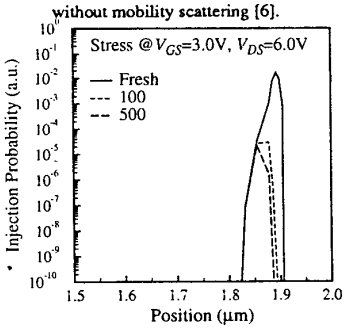

Fig. 6 The simulated injection probability for fresh and stressed devices.

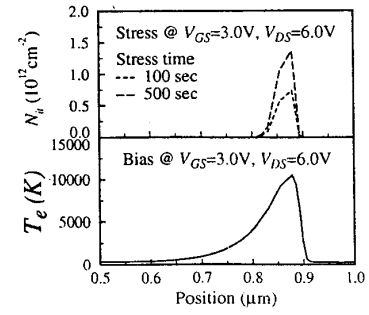

Fig. 4 The characterized spatial distribution of interface states for 100 and 500 sec stress. The calculated electron energy is also shown.

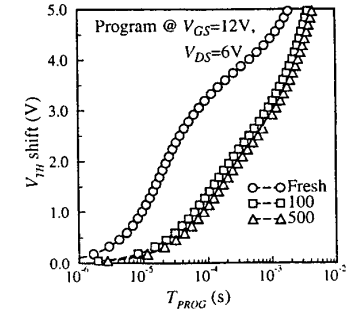

Fig. 7 The transient characteristics of the EPROM device before and after the stress. With increasing N_{it}, programming time is longer.