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# Analytical Current Conduction Model for Accumulation-Mode SOI PMOS Devices

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## Abstract

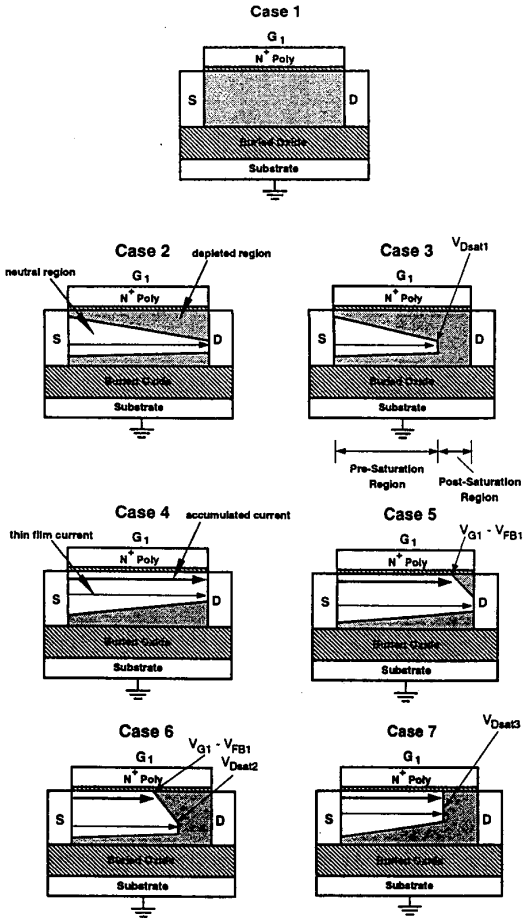
This paper reports a compact analytical current conduction model for short-channel accumulation-mode SOI PMOS devices. Based on the study, the current conduction mechanism in a short-channel accumulation-mode SOI PMOS device is different from that in a long-channel one. As verified by the experimental data, the compact analytical model considering channel length modulation and prepinchoff velocity saturation gives an accurate prediction of the drain current characteristics.

## Summary

Accumulation-mode SOI PMOS devices have advantages for VLSI applications[1][2]. Analysis of accumulation-mode SOI MOS devices have been reported [3]. But most of the analytical models are for accumulation-mode SOI MOS devices operating at a certain condition [4]. In this paper, an analytical drain current model considering channel length modulation and prepinchoff velocity saturation for short-channel accumulation-mode SOI PMOS devices is described. The differences between the short-channel analytical model and the long-channel one for the accumulation-mode MOS devices will be described.

The accumulation-mode SOI PMOS device under study has a $2 \times 10^{16}\text{cm}^{-3}$ p-type thin film of 1000Å above a 3500Å buried oxide. The p-type substrate doping density is $1 \times 10^{15}\text{cm}^{-3}$. A front thin oxide of 125Å is placed under an N+ polysilicon gate. Fig. 1 shows the mechanism of the conducting current in an accumulation-mode SOI PMOS device. The neutral thin film region may offer holes for current conduction. In addition, the accumulated holes at the top surface may also contribute to the mobile carriers for current conduction. Depending on the biasing condition, there are seven cases for the current conduction condition in the accumulation-mode SOI PMOS device as shown in Fig. 1. In Case 1, at a small $V_{G1}$, the thin film is fully-depleted for the device biased in the subthreshold region. In Case 2, as the magnitude of $V_{G1}$ increases, the upper and the lower portions of the thin film are depleted. Only the center portion of the thin-film is neutral, which can be provided for current conduction. In Case 3, the center conducting channel is pinched off. In Case 4. as the magnitude of $V_{G1}$ further increases, the top depletion region disappears. The neutral region spreads from the center to the top. In addition, holes accumulated at the top surface. The current conduction is via the neutral region and the accumulated hole region at top. If the magnitude of $V_D$ increases, as shown in Case 5, the top hole-accumulated channel is pinched off. Beyond the top pinchoff point, the center neutral region is more important for current conduction. If the magnitude of $V_D$ increases further, even the center neutral region may pinch off as shown in Case 6. In Case 7, the top and the center channels may reach the saturation point at the same lateral location. This means that both the top accumulated and the center neutral channels are equally important for current conduction at this location. Compared with the current conduction in the long-channel accumulation-mode SOI MOS devices, Case 7 for the short-channel accumulation-mode SOI PMOS device is unique. Prepinchoff velocity saturation may exist in the top accumulated channel. In Case 2, since the drain end of the center channel is not pinched off, the drain current for Case 2 is expressed as Eq. (1) in Fig. 2. In Case 4, the top surface may have accumulated holes. The accumulated surface channel at top is not pinched off. In addition, the hole velocity in the center neutral channel does not reach the saturated velocity. The drain current for Case 4 is Eq. (2). In Case 5, the center neutral channel does not have the post-saturation region and the drain current for Case 5 is Eq.(3). The models for other cases can be similarly obtained [5]. Fig. 3 shows the judgment flowchart for determining which drain current formula should be used for the accumulation-mode SOI PMOS device. As shown in the figure, if $V_{G1} > V_{TH}$, the device is biased in the subthreshold region, Case 1 drain current formula should be used. If $V_{G1} < V_{TH}$, a further decision is necessary. If $V_{G1} - V_{FB1} > 0$, Case 2 and Case 3 formulas should be used. If $V_D > V_{Dsat1}$, Case 2 formula should be used. Otherwise, Case 3 formula is used. If $V_{G1} - V_{FB1} < 0$, a further decision is necessary. If $V_{G1} - V_{FB1} > V_{Dsat2}$, Cases 4,5,and 6 should be used. Otherwise, Cases 4 and 7 should be used. Fig. 4 shows the drain current vs. the drain voltage of the accumulation-mode SOI PMOS device based on the analytical model considering velocity saturation and channel length modulation and the experimental data [2]. Without considering channel length modulation, substantial deviations can be seen in the saturation region. Without considering velocity saturation, the drain current in both the triode and the saturation regions is overestimated. As shown, a good correlation between the model result and the experimental data can be seen. Fig. 5 shows the drain current vs. the front gate voltage of the accumulation-mode SOI PMOS device based on the analytical model and the experimental data [2]. As shown in the figure, as $|V_{G1}|$ is large enough, the device is operating in Case 4 for a small $|V_D|$ and in Case 7 for a large $|V_D|$. As $|V_{G1}|$ is small, the device is operating in Case 1 (subthreshold). In transition, the device is operating in other cases. As shown in the figure, the transition region is more complicated for a small $|V_D|$.

[1] O.Faynot et.al., *IEEE TED*, pp.713 4/95.
[2] L.Wang, et.al., *IEDM Tech. Dig.*, pp.679 91.
[3] A.Terao, et.al., *IEEE EDL*, pp.682, 12/91.
[4]D.Flandre,A.Terao, *Solid-St Elec*, pp.1085 8/92.
[5] J. Kuo et.al., *IEEE TED*, pp.755 93.




$$I_{D2} = \frac{W}{L_{eff}} \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}} \frac{V_D}{L_{eff}}} q N_{si} t_{si} [V_D + F_1(V_D) - F_1(0) + F_2(V_D) - F_2(0)] \quad (1)$$

$$F_1(V) = \frac{C_{si}}{C_{ox1}} V + \frac{q N_{si} t_{si}^2}{3\epsilon_{si}} [(\frac{C_{si}}{C_{ox1}})^2 + \frac{2\epsilon_{si}}{q N_{si} t_{si}^2} (V_{G1} - V_{FB1} - V)]^{\frac{3}{2}}$$

$$F_2(V) = \frac{C_{si}}{C_{ox2}} V + \frac{q N_{si} t_{si}^2}{3\epsilon_{si}} [(\frac{C_{si}}{C_{ox2}})^2 + \frac{2\epsilon_{si}}{q N_{si} t_{si}^2} (V_{Geff2} - V_{FB2} - V)]^{\frac{3}{2}}$$

$$I_{D4} = -\frac{W}{L_{eff}} C_{ox1} \frac{\mu_{s0}}{1 - \frac{\mu_{s0}}{v_{sat}} \frac{V_D}{L_{eff}}} [(V_{G1} - V_{FB1}) V_D - \frac{1}{2} V_D^2] + \frac{W}{L_{eff}} q N_{si} t_{si} \cdot \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}} \frac{V_D}{L_{eff}}} [V_D + F_2(V_D) - F_2(0)] \quad (2)$$

$$I_{D5} = -\frac{W}{L_{eff}} \frac{\mu_{s0}}{1 - \frac{\mu_{s0}}{v_{sat}} \frac{V_D}{L_{eff}}} \frac{1}{2} C_{ox1} (V_{G1} - V_{FB1})^2 + \frac{W}{L_{eff}} \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}} \frac{V_D}{L_{eff}}} q N_{si} t_{si} \cdot [V_D + F_1(V_D) - F_1(V_{G1} - V_{FB1}) + F_2(V_D) - F_2(0)] \quad (3)$$

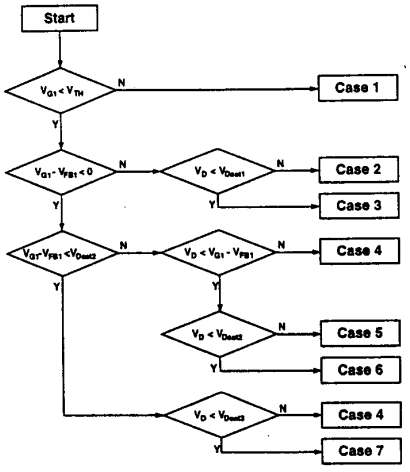
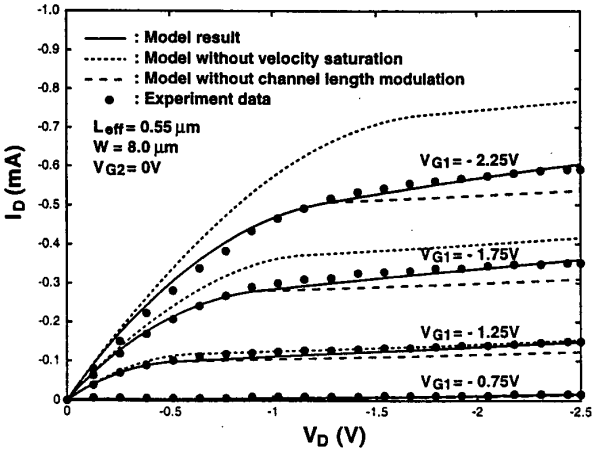



Fig. 1. Various current conduction mechanisms in the accumulation-mode SOI PMOS device biased at various conditions.
Fig. 2. Important equations.
Fig. 3. Judgment flowchart for determining which drain current formula should be used.



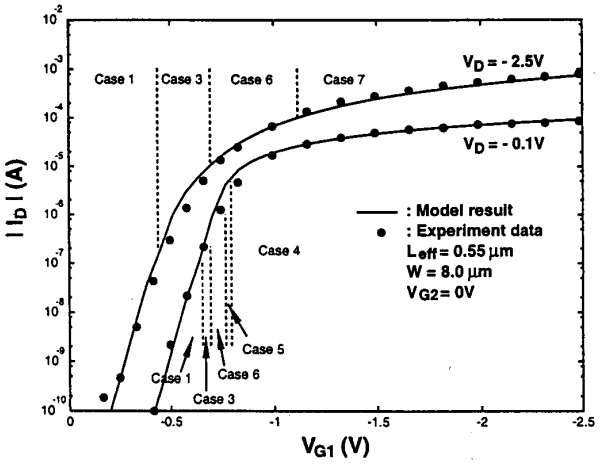




Fig. 4. The drain current vs. the drain voltage of the accumulation-mode SOI PMOS device based on the analytical model considering velocity saturation and channel length modulation and the experimental data [2].
Fig. 5. The drain current vs. the front gate voltage of the accumulation-mode SOI PMOS device based on the analytical model and the experimental data [2].