P–16

Two-Dimensional Calibration of Dopant Transport Models for Submicron CMOS Transistors

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Introduction: In most cases complex process models for Damage Enhanced Diffusion (DED) are calibrated from one-dimensional measurements (vertical SIMS or spreading resistance). MOS transistors in the submicron regime however are inherently two-dimensional devices. In this paper we analyse, whether a one-dimensional calibration of an advanced DED model is sufficient for a correct lateral subdiffusion of the source/drain dopants /1,2/.

Measurements: Following the CMOS process flow SIMS measurements have been performed for p-well, n-well, anti punch doping, channel doping and source/drain doping (Fig.1). This was done for p- and n-MOSFET, respectively at as implanted condition and at the end of the process flow. The short channel behaviour of MOSFETs is very sensitive to the source/drain subdiffusion (Fig.1). Thus we measured the threshold voltage as a function of the gate length $U_{th}(L_g)$ and compared them with corresponding device simulations based on the doping profiles under investigation.

Process Models and Simulation: For the simulations we used TSUPREM4 (process) and MEDICI (device) from TMA, Inc.. During the source/drain implants damage was created by the "plus one" model. The amount of damage was controlled by the parameter *d.plus* (Fig.1). After source/drain implants the extrinsic pair diffusion model *pd.full* was used during annealing. This model accounts for kick-out type reactions, Frank-Turnbull type reactions and for interstitial-vacancy recombination.

Calibration Results: In a first step all as implanted profiles have been compared to SIMS. For p^+ and n^+ minor corrections of the distribution moments were necessary to get agreement (Fig.2a,b,c). In a second step all profiles at the end of the process flow have been compared to SIMS (Fig.2a,b,c). Using the diffusion model *pd.full* the parameter *d.plus* in the implant damage model was varied to get the correct diffusion into the depth. In a third step two-dimensional MOS structures have been created. For these MOSFETs the $U_{th}(L_g)$ characteristics have been calculated with MEDICI. To achieve agreement with measurements (Fig.3a,b) *d.plus* and the segregation coefficients *seg.0* (for boron in the n-MOSFET and for phosphorus in the p-MOSFET) have been varied. The U_{th} roll-off has been modified by *d.plus* via the source/drain subdiffusion (Fig.1). U_{th} at large gate lengths has been modified by *seg.0* via the surface concentration in the channel region (Fig.1). A rough value for *d.plus* was found from SIMS and a fine calibration was found from the U_{th} roll-off.

d.plus and *seg.0* are the only model parameters, that have been changed from default values. Both parameters are not independent from each other because the implant damage diffuses into the channel region. The main advantage of this calibration strategy is that p- and n-MOSFET can by calibrated independently without losing physical consistency: The damage from the source/drain implants is different in p- and n-MOSFETs. Transport coefficients for defects or dopants however should be the same in p- and n-MOSFETs.

Usually for application simulations CPU-time is minimized. If no inconsistency with experimental data occurs the model complexity is chosen as low as possible. Thus the same procedure (step 1-3) was repeated with the most simple diffusion model *pd.fermi*. All SIMS profiles can be callibrated with *pd.fermi* too. However, the subdiffusion is to large (Fig.3a,b). The reason is that the defect concentration close to the surface is much lower than in the area of the source/drain vertical junctions (Fig.4). Thus source/drain dopants can move faster into the depth than into the lateral channel area.

Conclusion: A phasically based calibration strategy is proposed which regards consistently for vertical SIMS and lateral short channel behaviour as well as for p- and n-MOSFETs.

References: /1/ N.E.B.Cowern; J.Appl.Phys. **64** (9), p.4484, 1988
/2/ M.E.Law, J.R.Pfiester; IEEE ED-**38** No.2, p.278, 1991

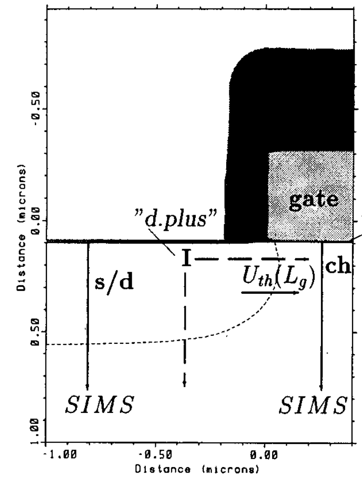

Fig.1: Schematic view of measurements: vertical SIMS for source/drain (s/d) and channel (ch), lateral $U_{th}(L_g)$ for source/drain subdiffusion.

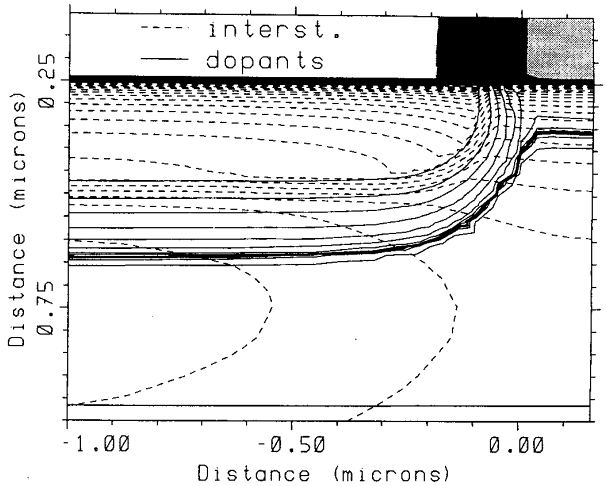

Fig.4: Distributions of dopants and interstitials in the p-MOSFET.

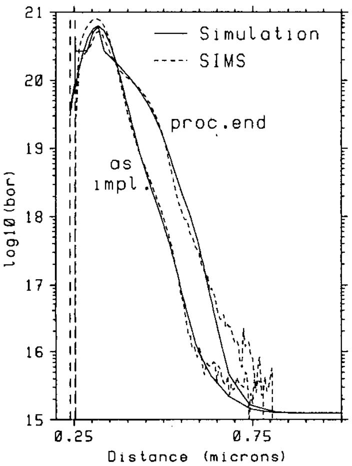

Fig.2a: Vertical boron distribution in the source/drain area of the p-MOSFET.

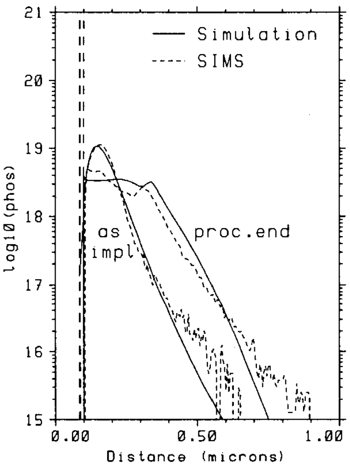

Fig.2b: Vertical phosphorus distribution in the source/drain area of the n-MOSFET.

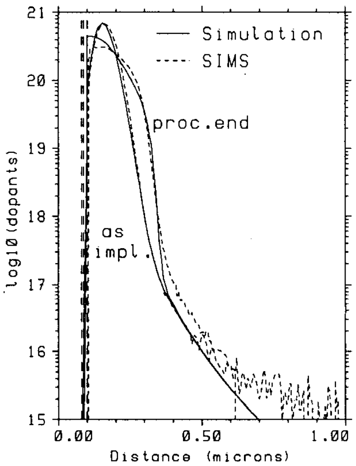

Fig.2c: Vertical arsenic distribution in the source/drain area of the n-MOSFET.

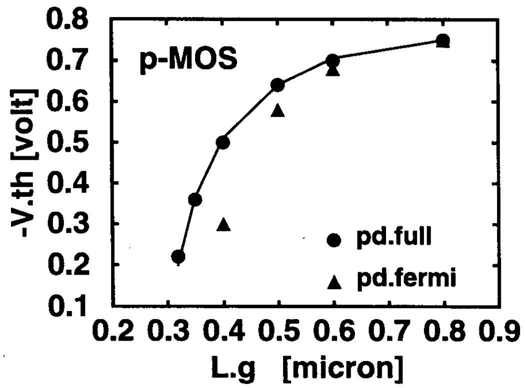

Fig.3a: Threshold voltage as a function of the gate-length for p-MOSFET (measured: line; simulated: symbols).

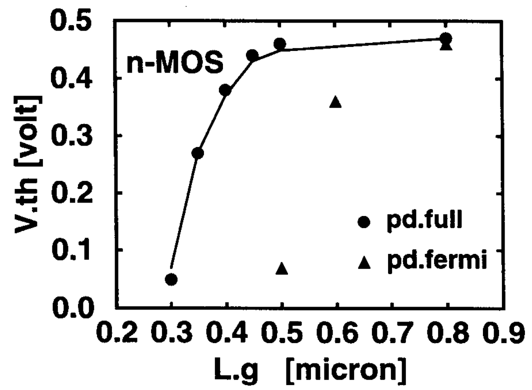

Fig.3b: Threshold voltage as a function of the gate-length for n-MOSFET (measured: line; simulated: symbols).