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Soft Error Rate Modeling and Analysis of SOI/TFT SRAM's

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Introduction. Although SRAM's built in SOI or with TFT's are known to be less prone to soft errors than SRAM's built on bulk material [1], it has been seen that α–particle generated charge in the channel region of an SOI transistor can cause the channel–source junction to become forward biased [2]. The forward biasing of this junction causes charge to be injected into the channel and appears as drain current. Figure 1 shows device simulation results for a $1.0\mu m$ channel length SOI NMOS transistor of the time evolution of the channel potential after an α–particle strike in the channel. It is clearly seen that it takes a long time for the channel potential to relax back to its equilibrium value. Essentially, a parasitic bipolar transistor with the channel acting as base, source acting as emitter, and drain acting as collector, is causing the α–particle generated charge to be multiplied by the gain of the bipolar transistor, where gain as defined here is the ratio of the time integral of the drain current to the α–particle induced channel charge for an "OFF" transistor. This effect occurs in TFT's as well as SOI MOS transistors.

Gain Control and Variations in SOI/TFT Devices. Simulations and experiments show that there are a myriad of methods to control the gain of the parasitic bipolar transistor [3], but one of the largest factors controlling the gain is channel length (base width). Device simulations of an α–particle strike in an SOI MOS transistor show that the gain increases at a rate much faster than the expected $\frac{1}{L_{eff}}$ dependence of a bipolar transistor. As MOS channel length decreases, we would expect to see that an SRAM built on SOI or with TFT transistors will become more susceptible to soft errors.

Simulation of Soft Error Rate. A charge generation/collection model for SOI/TFT SRAM's was incorporated into the Soft Error EValuator, *SEEV*[4]. *SEEV* uses Monte Carlo methods to determine the soft error rate (SER) of a circuit. Soft Error Rates were simulated using SEEV for a typical $0.35\mu m$ channel length 6T bulk SRAM and for the same 6T SRAM built on SOI. Figure 2 shows the results of these simulations. For a given SRAM cell, the critical charge (Q_{crit}) is the amount of charge required to cause the SRAM cell to switch states after an α–particle strike.

Estimates of Maximum Allowable Gain. Circuit simulations indicate that Q_{crit} for the bulk SRAM cell is $\approx 95fC$. For this value of Q_{crit}, *SEEV* estimates the SER to be $\approx 5.0 \times 10^{-5} errors/cell/\alpha$, as seen in Figure 2. For the SOI SRAM cell, circuit simulations tell us that Q_{crit} decreases to $\approx 32fC$ due to lesser amounts of parasitic capacitance. *SEEV* SER estimates were performed for the SOI SRAM with the parasitic bipolar gain equal to one. For a gain of one, Figure 2 shows that we would expect to see that the SER for the SOI SRAM is not measurable. If we consider a non–unity value for the gain of the parasitic bipolar transistor, the SER for the SOI SRAM cell will tend to be larger for a given value of charge collected (Q_{coll}). In essence, Q_{coll} will be multiplied by the gain of the TFT/SOI transistor. Figure 3 shows this effect of scaling the collected charge by a gain of 10.

We can now define the maximum allowable gain of an SOI/TFT device as the gain of a parasitic bipolar transistor that will cause the SOI/TFT SRAM SER to be the same as that of a bulk SRAM cell. Because the SER estimate for the bulk SRAM was determined to be $\approx 5.0 \times 10^{-5} errors/cell/\alpha$, we find that *SEEV* estimates the SER for the SOI/TFT cell to be $\approx 5.0 \times 10^{-5} errors/cell/\alpha$ for a Q_{coll} value of $3.2fC$ with unity gain. Because Q_{crit} for the SOI/TFT cell is $\approx 32fC$, we determine the maximum allowable gain for the SOI/TFT device to be $G_{max} = \frac{\approx 32fC}{3.2fC} = 10$. As long as the

maximum allowable gain of parasitic bipolar transistor in an SOI/TFT device is kept less than 10, the SER of an SOI/TFT SRAM cell will be less than that of the same design of a bulk SRAM cell.

Design Considerations. This paper will address methods to increase the maximum allowable gain including lifetime reduction, decreasing SOI film thickness and increasing the channel doping. The effect of lowered power supply voltages on the gain of the parasitic device and ramifications of that to the SER of SOI SRAM's will also be discussed.

Bibliography.

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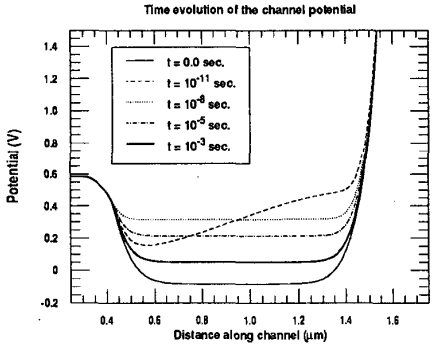

Figure 1. Evolution of the channel potential in a $1.0\mu m$ channel length SOI transistor as a function of time. At short times, we see that the gradient of the channel potential causes the injected carriers to be collected very quickly.

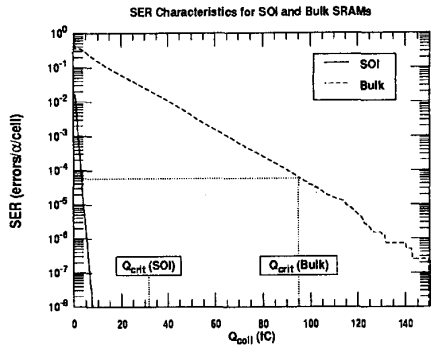

Figure 2. Comparison of SOI and BULK SRAM SER characteristics. For the bulk SRAM structure considered here, the critical charge is $\approx 95fC$ while it is only $\approx 32fC$ for the SOI SRAM cell.

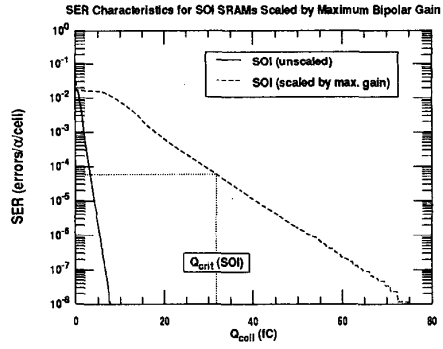

Figure 3. Results of scaling the SER of the SOI SRAM by the maximum allowable gain. Because the parasitic bipolar transistor in the SOI structure multiplies the collected charge, the unscaled SER characteristics are expanded along the ordinate by the gain factor.