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Robust simulation for the hysteresis phenomena of SOI MOSFET's by Quasi-Transient Method

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Introduction

Device simulation of SOI(Silicon On Insulator) MOSFET's has several difficulties originating from the floating body features. One of them is numerical unstability of solution of carrier densities in channel region due to the floating body effect, which is unlike the conventional MOSFET's. Another problem is physical possibility of multiple solutions at even the same bias condition, which results in the hysteresis characteristics such as Single-Transistor Latch(STL) phenomena[1]. To improve robustness of SOI simulation, we have developed a Quasi-Transient(QT) method for static(DC) mode analysis, and showed that fast and stable DC analysis is realized in device simulation of SOI MOSFET's[2].

In this paper, we show that the STL phenomena of SOI MOSFET's are successfully simulated with the QT method for analizing floating body and parasitic bipolar effects of thin-film SOI devices.

Quasi-Transient Device Simulation and its Robustness

Figure 1 shows a general flow-chart of the Quasi-Transient device simulation. In the QT simulation, a solution of former bias condition is used as the initial guess for a new bias condition, as is in the conventional method. Calculation is carried out, however, with formulation of transient analysis by Newton's iterative method. Δt is gradually increased as the iterative loops are processed, and finally, the DC formulae with condition of $\Delta t \rightarrow \infty$ are calculated, so that we can obtain the solution for the new bias condition.

Advantages of this QT simulation are as follows,

1) The matrix becomes diagonally dominant as desired with the transient formulation using small Δt.
2) Stable simulation is realized even for an abrupt bias change.
3) The multiple solution is naturally obtained in such hysteresis phenomena like SOI devices.

Figure 2 compares convergence efficiency of the QT simulation with the conventional static simulation. Here, the simulations were carried out with a solution of V_{DS}=0.5[V] and V_{GS}=0.5[V] as the initial guess to solve the status of V_{GS}=1.0[V]. Details of simulated device are summerized in table 1.

The QT results show shorter calculation time in each iteration of linear solution than the conventional method. The QT results also show a stable solution of carrier densities, while the conventional method obtains non-realistic solution with negative carrier densities, or even can not converge in MEDICI[3].

Device Simulation of Single-Transistor Latch Phenomena

Figure 3 shows simulated I_d-V_{gs} characteristics of SOI MOSFET. At higher drain voltage, V_d=1.0[V], the STL phenomena is observed. In positive sweep (V_{gs} is increased from 0.1[V] to 1.5[V]), drain current, I_d, increases steeply in the subthreshold region and MOSFET turns on about V_{gs}=0.0[V]. In negative sweep (V_{gs} is decreased from 1.5[V] to −1.0[V]), I_d decreases on the same curve as positive sweep in 'ON' region until V_{gs} is about 0.0[V]. The curve splits, however, below V_{gs}=0.0[V] by the floating body effects. In lower V_{gs} region (below −0.1[V]), holes accumulated in channel(base) region turn-on the parasitic bipolar transistor so that I_d increases as V_{gs} decreases.

Figure 4 shows generation and recombination rates in SOI layer at V_{ds}=1.0[V] and V_{gs}=−0.1[V] in both positive(a) and negative(b) sweep. The QT simulation shows robustness in the hysteresis of device status at the same bias condition.

Conclusion

In this paper, we have demonstrated robustness of the Quasi-Transient method for solving thin-film SOI MOSFET's. With the QT simulation, Single-Transistor Latch phenomena with hysteresis I_d-V_{gs} characteristics were successfully obtained in DC analysis.

It is expected that multiple status for the same bias such as thyristors are also simulated using the QT method.

References

[1] C.E.D.Chen, M.Matloubian, R.Sundaresan, B.Y.Mao, C.C.Wei and G.P.Pollack, "Single- Transistor Latch in SOI MOSFET's," *IEEE EDL*, vol.9, pp.636-638, Dec. 1988.

[2] R.Ikeno and K.Asada, "Stable Solution for SOI MOSFET Simulation by Quasi-Transient Method," 43rd Spring Meeting of Japan Society of Applied Physics , 26p-H-3, Mar. 1996.

[3] "TMA MEDICI Two-Dimensional Device Simulation Program," Technical Modeling Associates, Inc.

Table 1: Simulated Device Parameters

Type	n-type,single drain
L_g	0.6[μm]
N_A	2.0×10^{17}[cm^{-3}]
N_D	1.0×10^{19}[cm^{-3}]
T_{fox}	8[nm]
T_{SOI}	50[nm]
T_{box}	50[nm]
# of grids	54×27

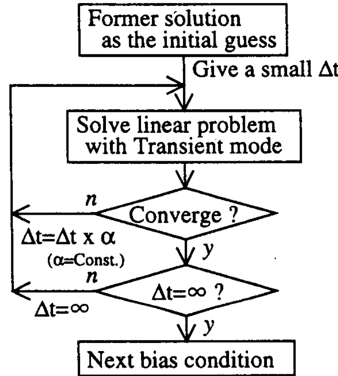


Figure 1: Flow-chart of Quasi-Transient method

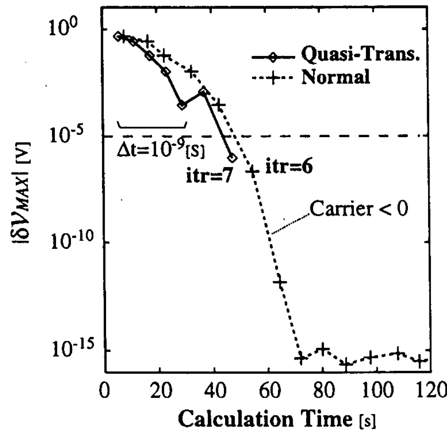


Figure 2: Comparison of convergence efficiency, solid-line : QT, dashed-line : conventional, (V_{ds}=0.5[V], V_{gs}:0.5→1.0[V])

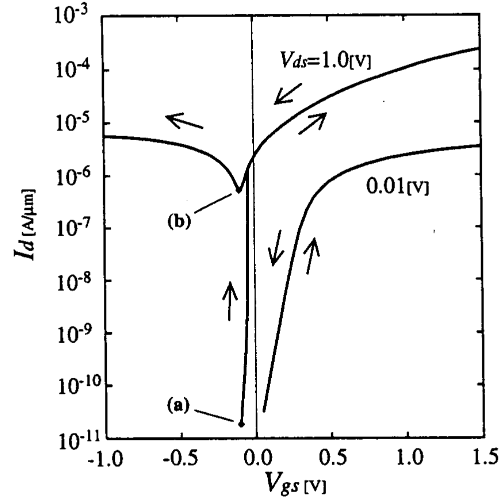
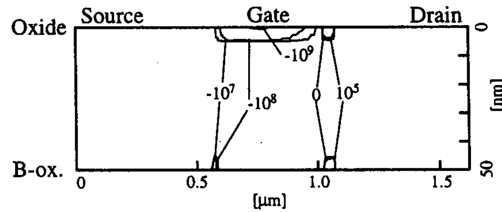
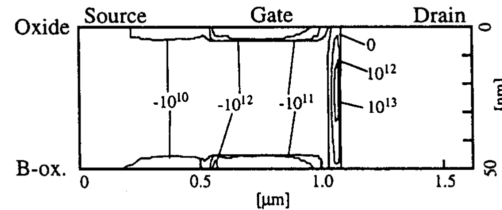


Figure 3: Simulated I_d-V_{gs} characteristics of n-type SOI MOSFET (V_{ds} as parameter). (a) and (b) are coresponding these in Fig.4



(a) positive sweep



(b) negative sweep

Figure 4: Generation (+) and recombination (−) rate in SOI layer [cm^{-3}s^{-1}] (V_{ds}=1.0[V], V_{gs}=−0.1[V])