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Application of LE-FDTD method to HF circuit analysis

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In this abstract, a circuit simulation technique is discussed, which accounts for the "full-wave" analisys of signal propagation along the interconnections of an arbitrary circuit, including active, non-linear devices. A number of electromagnetic propagation effects have indeed significant influence over high-frequency (either analog or digital) circuit performances, and can be accurately modeled by means of the approach described in the following: among them, interconnection behavior, cross-talk phenomena, package interactions. Conventional circuit CAD tools allows for the analysis of such effects by resorting to equivalent-circuit, lumped-element descriptions of interconnecting lines. Although this technique being highly computationally efficient, the definition of the equivalent circuit topology and the estimation of its parameters often relies on rather drastic approximations, because of the inherently "distributed" nature of most propagation effects. To tackle this problem, the Lumped-Element, Finite-Difference Time-Domain (LE-FDTD) technique has been conceived. Within this approach, SPICE-like compact device models are coupled to the numerical solution of Maxwell's equation over distributed domains. In this abstract, the extension of LE-FDTD technique to circuits including GaAs MeSFET devices is reported, and a few simulation examples are illustrated.

The FDTD integration scheme for Maxwell's equations was introduced by Yee [1] in 1966. The extension to lumped elements has been devised by Sui *et al.* [2]: to this purpose, an additional term $\vec{J}_{cl}$, representing the current flowing across the lumped device, is incorporated into the conduction current term $\vec{J}_c$ appearing in Maxwell curl-H equation:

$$\mathrm{rot}\vec{H} = \epsilon\frac{d\vec{E}}{dt} + \vec{J}_c \qquad , \qquad \vec{J}_c = \vec{J}_{cd} + \vec{J}_{cl}.$$

Maxwell's equations are discretized over a 3D, orthogonal grid, whereas current contributions coming from compact device models are ascribed to the cell(s) at which the device is placed. Details about numerical treatment of such equations have been given elsewhere [3]. Several device models have been included into the code: linear elements, such as voltage sources, resistors, capacitors and inductors, as well as non linear ones (non-ideal pn and Schottky junctions, BJT, GaAs MeSFET). To illustrate the discretization procedure, let us refer to the GaAs MeSFET: its model is obtained by assembling a network of sub-elements, according to the equivalent network proposed by Curtice [4]. The basic contribution to the drain current, following the so-called "quadratic" formulation (Curtice "cubic" expression has been implemented as well) , reads:

$$I_{ds}\left(V_{ds}, V_{gs}(1-\tau)\right) = \beta(1+\lambda V_{ds})\left((V_{gs}-V_{to})^2 - 2\tau(V_{gs}-V_{to})\frac{dV_{gs}}{dt}\right)\tanh(\alpha V_{ds}) + \frac{V_{ds}}{R_{ds}} + C_{ds}\frac{dV_{ds}}{dt}$$

Sub-elements are lumped at adjacent FDTD cells, as shown in Fig. 1. E-field components are then integrated to provide the voltage drops applied at sub-element teminals. Following the "leapfrog" time-stepping procedure, device equations are solved, together with H-field components, at odd time intervals only, whereas E-field components (and thus device boundary conditions) are instead updated at even timesteps. According to Yee's notation, Eq. 1 can be given the following discrete form:

$$J_y^{n+\frac{1}{2}}\left(i, j+\frac{1}{2}, k\right) = \frac{\beta}{\Delta x\Delta z}\left(1+\lambda\Delta y\frac{E_y^{n+1}\left(i, j+\frac{1}{2}, k\right) + E_y^n\left(i, j+\frac{1}{2}, k\right)}{2}\right)\cdot$$

$$\cdot\left(\left(\Delta x\frac{E_x^{n+1}\left(i+\frac{1}{2}, j+1, k\right) + E_x^n\left(i+\frac{1}{2}, j+1, k\right)}{2} - V_{to}\right)^2 -\right.$$

$$\left.-2\tau\left(\Delta x\frac{E_x^{n+1}\left(i+\frac{1}{2}, j+1, k\right) + E_x^n\left(i+\frac{1}{2}, j+1, k\right)}{2} - V_{to}\right)\right)\cdot$$

$$\cdot\tanh\left(\alpha\Delta y\frac{E_y^{n+1}\left(i, j+\frac{1}{2}, k\right) + E_y^n\left(i, j+\frac{1}{2}, k\right)}{2}\right) +$$

$$+\frac{C_{ds}\Delta y}{\Delta x\Delta z}\frac{E_y^{n+1}\left(i, j+\frac{1}{2}, k\right) - E_y^n\left(i, j+\frac{1}{2}, k\right)}{\Delta t} + \frac{\Delta y}{\Delta x\Delta z}\frac{E_y^{n+1}\left(i, j+\frac{1}{2}, k\right) + E_y^n\left(i, j+\frac{1}{2}, k\right)}{2R_{ds}}$$

to be inserted into the discretized expression of (1). Similar schemes hold for different devices: the resulting solution strategy allows for analyzing the field propagation within arbitrary circuits, accounting for actual behavior of non-linear components. A first simulation example is shown in Fig. 2, and consists of the time response of a simple GaAs MeSFET, common-source amplifier, operating in the microwave range. The plot compares input and output signals when the amplifier is working in the non-linear regime; the influence of connection-line and parasitic reactances is made evident by the phase shift and by the uneven behavior of rising and falling edges of the output signal. A more demanding simulation is illustrated in Figs. 3 and 4, which refer to the analysis of crosstalk occurring between

neighbouring lines in a multi-chip module circuit. Line terminate at ECL digital gates, the input and output stages of which are accounted for in the simulation. A 1 ns pulse travels along one line: the corresponding crosstalk noise computed at the end of the neighboring line is shown in Fig. 4, which also illustrates the regenerating action of the differential pair Q_2, Q_3. Finally, the layout of a GaAs-MMIC, consisting of a Traveling-Wave Amplifier (TWA), is shown in Fig. 5. The circuit, which employs five MeSFET devices and inherently exploits wave propagation effects, represents a significant test case for the simulation technique described so far. A detailed discussion of such simulation results is beyond the scope of this abstract: in Fig. 6, just a plot of the E-field component normal to the circuit surface is shown, which makes it evident the influence of active devices (the larger peaks in the foreground). Lower peak at background are instead located at the bent sections of the signal path.

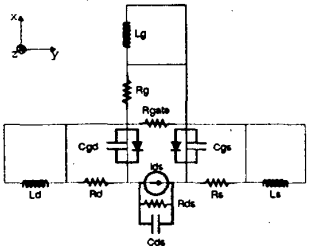

Fig. 1

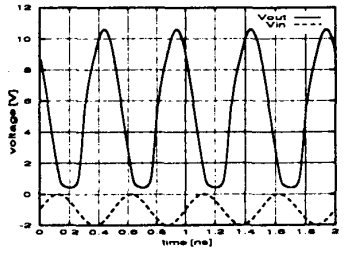

Fig. 2

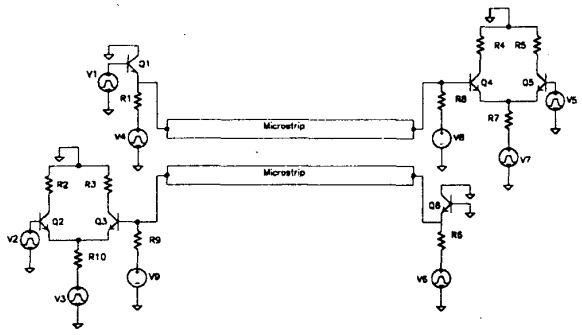

Fig. 3

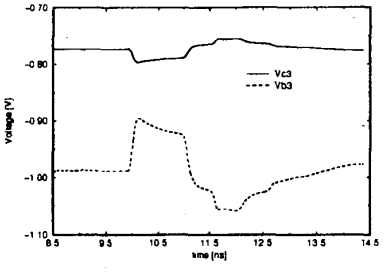

Fig. 4

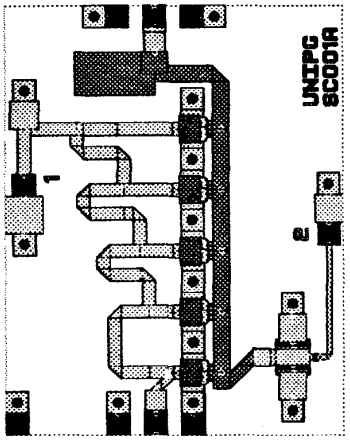

Fig. 5

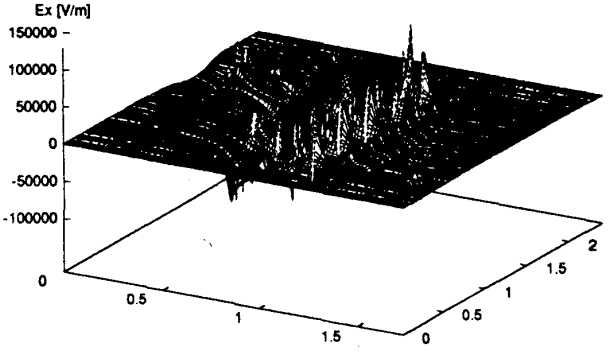

Fig. 6

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[2] W. Sui *et al.*, *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 724–730, 1992.
[3] P. Ciampolini *et al.*, *MTT Intl. Sym. Digest*, vol. 2, pp. 361–64, 1995.
[4] W.R. Curtice, *IEEE Tran. Trans. Microwave Theory Tech.*, vol. 28, pp. 488–496, 1980.